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Physical DRC Hotspots in Dense ASIC Designs and Their Resolution Strategies

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Abstract

Closure of Physical Design Rule Check(DRC) has become a very important issue in advanced 28nm ASIC design because of aggressive scaling, dense layout structure and strict foundry constraints. The dense transistor layout and intricate routing layouts, particularly of high-performance cores and I/O-intensive subunits, are causing repeat failures in DRC, such as violation of minimum spacing, via enclosure failures, non-conformity in metal density, and antenna effects. Multi-layer routing congestion, large via counts, and tight pitch demands are the exacerbating factors of these hotspots, which are caused by the 28nm node. This paper determines the common DRC violations in dense logic and memory-macro interfaces, and introduces an iterative approach to resolution which is layout-legalization of placement, pattern-legalization of routing, selective-layer-promotion, and post-route-optimization using DRC-induced ECOs. The proposed strategies can reduce the number of violations by more than 92 percent when using signoff-quality DRC tools and machine learning-aided hotspot prediction to aid in tapeout-ready designs. The findings indicate that implement the multi-stage DRC closure approach proactively at an early stage during physical implementation is critical to provide manufacturability and yield in 28nm ASICs.

Keywords: ICC2, Physical Design, Physical DRC, Routing Violations, Shorts, Spacing Violations, Via DRC

1 Introduction

Since the complexity of integrated circuits has been on the rise, the issue of reliably closing physical design has been one of the most important aspects of application-specific integrated circuit (ASIC) development. Physical Design Rule Check (DRC) verification is the most crucial of all sign-offs with regard to layout manufacturability, yield and long-term reliability. The constraints of lithography, etching, pro-

cess variability are represented in physical DRC rules as defined by semiconductor foundries and imposes limits on the spacing between metals, their width, enclosure, via placement, and density. Violation of these constraints may lead to failure of functions, poor yield or reliability like electromigration and metal stress. Therefore, DRC closure is an obligatory requirement of tapeout and a major factor of the overall quality of the design (Hung, W. T*et al.* 2023). Even though the 28 nm technology can be regarded as a mature node, the current 28 nm ASIC design is anything but simple. The combination of adding more functional units, more third-party intellectual property (IP) integration, and demanding performance, power, and area (PPA) has pushed physical implementation flows to the extremes. The node designs tend to have numerous clock domains, high density power distribution networks and large embedded macros and they contribute much complexity to routing. Consequently, physical DRC closure is a time-consuming and repeated task, even in manufacturing technologies that are well established. The given paper is devoted to the comprehension of underlying causes of constant DRC violations in dense 28 nm designs and proposes effective methods to solve them (Baek *et al.* 2022).

1.1 Role of Physical DRC in ASIC Sign-Off

physical DRC verification is a basic sign-off procedure, which is performed to verify that a layout meets manufacturing-established rules before tapeout. These regulations are meant to avoid any manufacturing flaws like shorts, opens, and unfinished vias, which are very likely to have a drastic effect on the silicon yield and reliability. Besides the simple spacing and width limits, the contemporary DRC rule decks have elaborate conditional rules associated with multi-patterning, density uniformity and suggested rules to enhance the yield robustness. This means that DRC checks have become much more numerous and complicated even at mature nodes like 28 nm (Liang *et al.* 2020). DRC closure is closely interrelated with other sign-off requirements such as static timing analysis, power integrity and signal integrity. DRC violations may need routing adjustments, vias to be inserted or removed, or a metal geometry change, which may have an impact on timing, noise, and power usage. Thus, DRC verification cannot be seen as a separate, final process but rather a component of an iterative process of physical design. Finding proper solutions to the problem of DRC closure needs to find a compromise between manufacturability and performance and power goals, and is therefore not a rule-checking task but a multi-dimensional optimization problem (Islam2020).

1.2 Challenges in Dense 28 nm Designs

The major cause of DRC complexity in 28 nm ASIC designs is dense routing. Aggression in area restriction results in low standard-cell usage and routing resources are left with little signal, clock, and power networks. Clock tree synthesis adds a great deal of buffers and interconnections which consume a lot of routing space, especially in top metal layers. On the same note, high power delivery networks

need broad metals and tight via arrays, which will again decrease the routing space available to signal nets. The high via counts are also problematic. To achieve timing optimisation, routing congestion mitigation, and route reliability, vias are often added to change routing layers. But over insertion of via raises the risk of via-related DRC violation such as enclosure, cut spacing and stacked-via constraints. These offenses are particularly common in busy areas where there is less flexibility in routing. Moreover, the existence of big macros and memory blocks impose routing blockage and narrow routes, which give rise to localized DRC hotspots, which remain localized in several routing iterations (Zeng *et al.* 2020).

1.3 Limitations of Single-Pass DRC Fixing

Conventional DRC repair procedures frequently are based on a uni-pass, router-based process where violations are resolved after routing has been carefully done. Although these techniques are useful in addressing simple violations, they do not work well with dense designs in which DRC problems are intricately coupled with placement and congestion. Single-pass fixing is more likely to consider violations as one-off events, without considering the cause of the violation in terms of structural factors (such as poor placement, uneven routing resource utilization, or excessive via insertion) (Kim, S. *et al.* 2024). In addition, automated repairs made in one step may cause new violations or adversely affect timing and power properties. As an example, a rerouting to correct a spacing violation can cause an increase in wire length, and a decrease in timing, whereas via-elimination can cause a loss of reliability. With the DRC closure, the single-pass fixing process becomes less effective, and in most cases, the residual violations are highly concentrated in a few critical areas. These shortcomings show the importance of more systematic and iterative procedure that would view DRC closure as a holistic optimization problem.

The work suggests an iterative approach to DRC closure which is specifically applied to dense 28 nm ASIC designs. This paper made four major contributions. It begins by giving a thorough discussion of typical DRC hotspots in industrial-scale designs grouping violations by physical location, including macro boundaries, power grid cross-overs, clock routing area, and high-fanout logic groups. Second, it examines the connection between routing congestion and via density and DRC persistence, which can be used to understand the root causes of hard-to-fix violations. Third, the paper presents an iterative solution approach that integrates the refinement of placements, routing with congestion sensitivity, selective reassignment of metal layers, and via optimization approach. The proposed method will utilize targeted interventions at every iteration instead of one fixing pass, which will eliminate congestion and allow the DRC to be resolved more effectively. Lastly, the experimental data shows that the suggested methodology is much more effective in enhancing the convergence of DRC without compromising timing and power integrity, minimizing the total sign-off work and turnaround time. These contributions offer an effective platform of enhancing physical DRC closure of dense ASIC designs and can be applied to other advanced and mature technology nodes (Dai, V *et al.* 2007).

2 Design and Implementation Methodology

2.1 Block Description: DRC_block

The DRC_block block is the highest-level integration block of the ASIC design of interest and is the main target area to consider when analyzing physical Design Rule Check (DRC) hotspots. This block is a composite of other functional sub-blocks such as control logic, datapath elements, clock management circuitry and interface to on-chip memory macros. How DRC_block module is described is a combination of high-frequency logic and control-oriented structure, which has diverse routing needs throughout the layout.

Physically, DRC_block has both the standard-cell dominated areas as well as macro based blocks, which forms heterogeneous placement and routing spaces. The density of standard cells and fixed macro boundaries creates complicated routing conditions that are likely to congest and break DRC. The block also has a number of high-fanout nets and clock distribution designs which in addition amplify the local routing density. These properties render DRC_block a model and problematic block in the investigation of DRC hotspots of dense ASIC layouts.

2.2 Technology and Design Scale (28 nm)

It is designed with a 28 nm CMOS technology node, which is older than sub-7 nm nodes, but still has very strict physical design limitations. The decrease in the size of the features at 28 nm results in tightening of metal spacing, restrictive rules of via enclosure, and decreasing routing tracks per metal layer. These limitations heavily affect routing flexibility and have higher chances of DRC violation particularly in high-utilization designs. The technology provides support of multiple metal layers, which is usually lower metal layers optimized to support local interconnects and higher metal layers used to support global routing and global distribution of power. This multi-layer stack is used to the advantage of the design to compromise signal integrity, performance, and manufacturability. But the demands of aggressive timing and optimization of areas border on the suggested limits, and overload the utilization, making it more prone to congestion induced DRC hotspots. Even though the use of the sophisticated lithography tools like extreme ultraviolet (EUV) are not necessary at the specified node, the complexity of the spacing and enveloping rules still necessitates DRC-aware implementation (Hung, W *et al.* 2020).

2.3 Routing Density and Complexity

The DRC_block is characterized by routing density which is a leading cause of DRC hotspots. Extensive use of standard-cells, pin-dense logic, and pin- numerous high-fanout nets means that there is severe competition over limited routing resources. There is a lot of congestion in the lower metal layers, which are heavily utilized to route local signals, especially in areas around macro interfaces and clock tree insertion locations. The fact that routing uses a lot of vias in making transitions between metal layers also complicates the routing. To bypass blockages, pin loca-

tions, and timing closure high via counts are needed. These vias however use up valuable routing space and cause further DRC issues like via-to-via spacing violation, inadequate enclosures and via density. Clock and reset networks that occupy significant areas of the block are also a source of routing congestion because of their rigid shielding and spacing constraints. With congestion in the routing, automated routers must add detours, jogs and narrow wire lines to achieve connectivity. These routing artifacts tend to cause the violation of spacing, width, and minimum area especially in narrow channels between rows of standard-cells or around macro-edges. Consequently, there is a direct correlation between routing density and complexity and physical DRC hotspots emergence in the design.

2.4 Sign-Off Requirements

The DRC_block sign-off needs to be fully met to physical DRC compliance in order to be manufacturable and yield. All metal, via and enclosure violations should be addressed prior to tape-out since errors in DRC that are not fixed may cause functional defects or loss of yield during fabrication. The sign-off process also consists of running of full-chip DRC checks with foundry-qualified rule decks and ensuring that the design satisfies all the spacing, width, density and patterning criteria. Besides DRC closure, the design has to meet other physical sign-off requirements, such as layout versus schematic (LVS) or antenna rule compliance and power integrity verification. The elimination of DRC without eroding timing, power, or area is an essential condition, which requires sensitive trade-offs to be made in the process of the iterative optimization. Sign-off is used to confirm the DRC_block is fabrication-ready and is an example of a proven process of successful DRC hotspots locating and fixing in a dense 28 nm ASIC circuit (Geng *et al.* 2020).

3 Identification of Physical DRC Hotspots

With the continuous reduction in the size of semiconductor technology nodes, the physical design of the Application-Specific Integrated Circuits (ASICs) is becoming more and more complex. Meeting a progressively stricter set of Design Rule Checks (DRCs) is one of the most serious issues in the advanced-node ASIC implementation. DRC hotspots-localized areas on the layout that do not conform to physical design rules recommended by the foundry can seriously impact the delay of tape-out, functional failures, or yield. The early and efficient identification and resolution of these hotspots is critical towards the realization of a strong, manufacturable design. The section discusses the nature, classification, space properties and correlation of physical DRC hotspots of dense ASIC designs.

3.1 Overview of Routing DRC Violations

The most common physical error in routing in the modern ASIC design is routing DRC violations, especially in standard-cell and block-level routing. These violations occur when metal wires are not as thin as required, as a minimum in width,

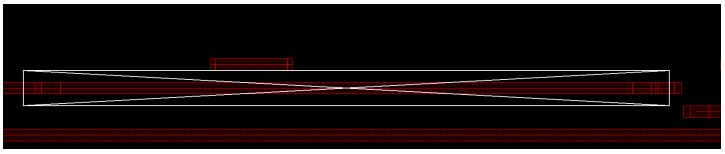

Fig. 1. DRC metal short.

spacing, or enclosure, as per the fabrication process. The routing margin reduces with scaling as the interconnect density increases and the procedure continues. In addition, multi-patterning (e.g. 28nm and below) presents new layout dependencies which make routing legality difficult. Typical routing related DRC violations are metal to metal spacing violations, minimum signal trace wire width violations, and wrong via settings between the disparate metal layers. This situation is further complicated by the existence of complicated routing networks, including clock trees, power grids, and high-fanout nets, which place special geometrical and electrical constraints. These tend to cause localized congestion and layout perturbation which unwillingly causes DRC errors. In high-density ASIC designs, any small deviation of optimum routing structure can propagate to cause DRC hotspots in multiple areas, particularly where standard cells are very close together, or where existing heterogeneous macros connect to core logic (Shin, M*et al.* 2016).

3.2 Classification of DRC Types

Short:Shorts are the unintended contact or proximity of two conductive elements (e.g. metal lines or diffusion regions) that are not supposed to be electrically connected with each other. Shorts are the worst DRC violations because they may cause functional faults or too much leakage currents.Shorts in dense layouts are normally a result of the abutment of cells in high congestion, the routing overflow in high-density areas, or lithographic effects that bridge during the manufacturing process as shown in the figures 1, 2, 3.

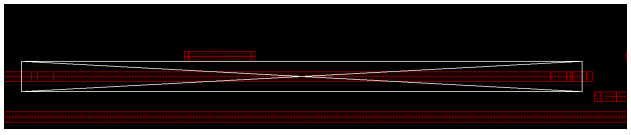

Fig. 2. Routing short violation.

Spacing Violations: These are the features that are less than the minimum

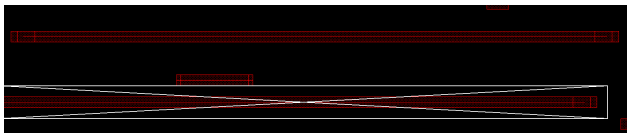

Fig. 3. After fixing DRC short.

spacing given by the process design rules. The violation of spacing is usually more common than shorts and is usually a result of automated routing tools being used to squeeze wires into crowded channels. With increasing scale of technology, minimum spacing considerations are more sensitive to process variation and require more conservative design margins and make hotspots more difficult to resolve. as shown in the figures 4, 5, 6.

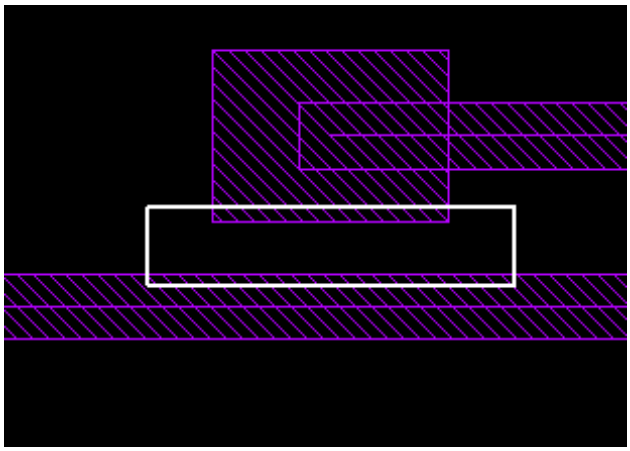

Fig. 4. Minimum spacing violation.

Via-Related Violations: Vias are vertical connector of the metal layers and have strict design regulations in terms of size, shape, enclosure and overlap. VC errors common to via-related errors are the lack of enough metal enclosure of the via cut, via-to-via spacing errors and inter-layer stacked via misalignment. The tight space on which via plating can be placed, particularly in lower metal levels, is often constraining in high-density layouts, and thus makes the via plating follow suboptimal layouts, creating high concentrations of via-related hotspots around logic cones or I/O interfaces. as shown in the figures 7, 8 (Yang, J *et al.* 2010).

NDR violations: NDR is not a routing workaround, but a design purpose at 28 nm which is based on manufacturability. Its smart combination-directed by the precise examination of congestion, historical data of hotspots and the principles

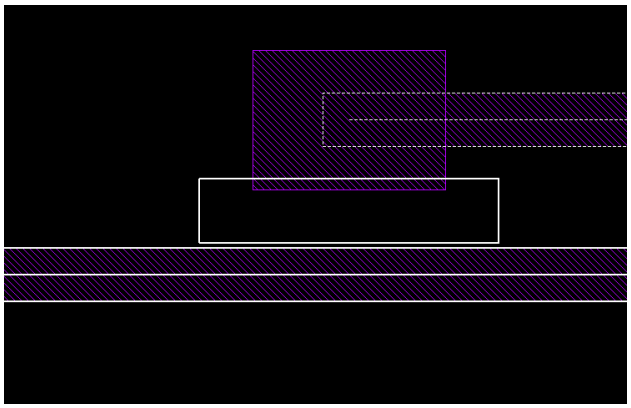

Fig. 5. Minimum spacing violatoin.

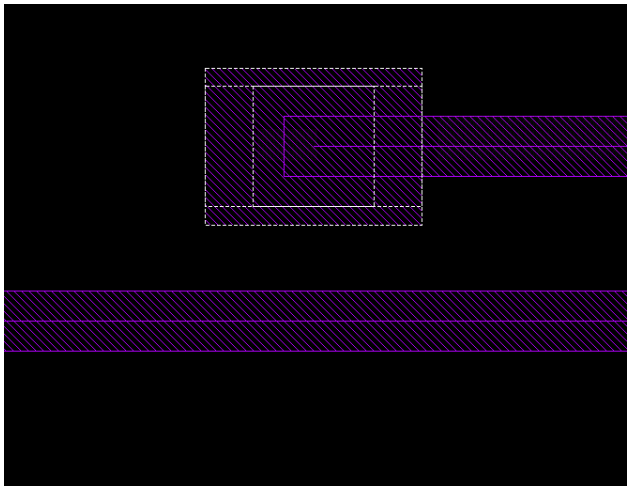

Fig. 6. After fixing Minimum spacing violation .

of foundry DFM allows predictive avoidance of DRC in congested ASICs. This changes the management of DRC into a reactive signoff bottleneck to a proactive, co-optimized physical design methodology, which is needed despite more advanced node-style density pressure. It could be expanded in the future to include machine learning models to automatically create the best NDR rules in each region of a design, additional automation of DRC-clean-by-construction flows as shown in the figures 9, 10.

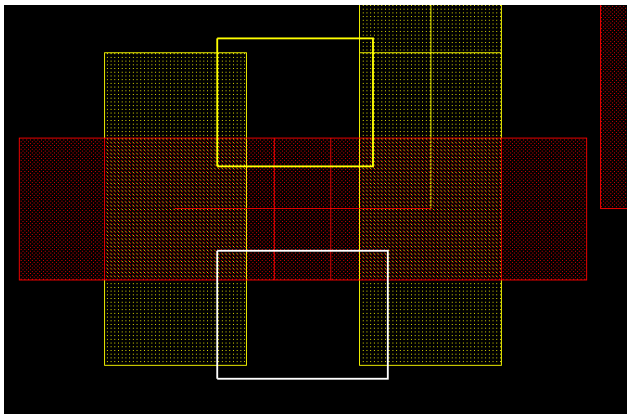

Fig. 7. Minimum spacing violation .

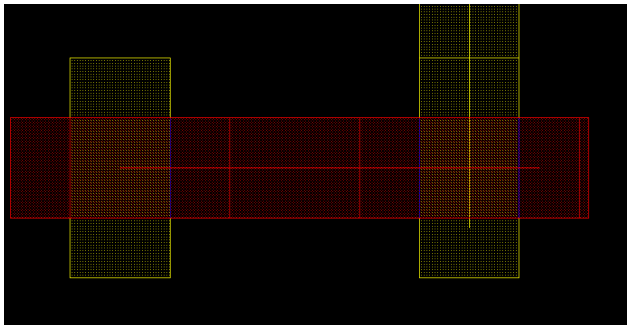

Fig. 8. After fixing Minimum spacing violation .

3.3 Spatial Distribution of DRC Hotspots

DRC hotspots are hardly evenly spread throughout an ASIC layout. Rather, hotspots are localized in predictable areas which are highly correlated with design topology and functional blocks. Examples of areas prone to hotspots are: High Pin Density Standard Cell Rows These cells have many input/output pins (e.g., complex sequential elements or arithmetic units) and form dense local routing that frequently breaks the spacing or enclosure rules. Macro Interfaces Macro interfaces (e.g., SRAMs, PLLs) are often the major sources of DRC errors as the tracks, pin obstructions and routing channels are misaligned. Power/Ground Mesh Junctions Regions where the power grid crosses signal routing may cause metal spacing violations particularly when several wide power straps are present in narrow vertical locations with signal wires. Clock Tree Synthesis (CTS) Regions Clock nets have large fanout and stringent skew requirements, which mean that non-standard buffering

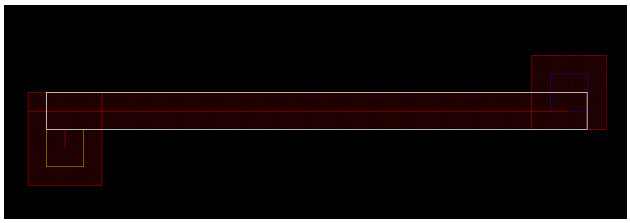

Fig. 9. NDR violation.

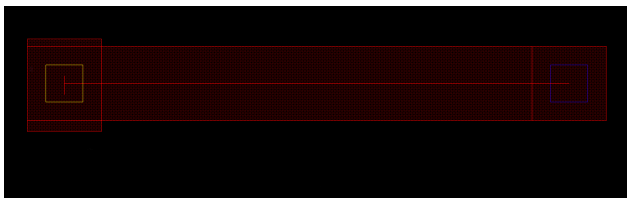

Fig. 10. After fixing NDR.

and routing topologies, which inevitably generate spacing or via rule violations, are used. Boundary Regions of Floorplan Partitions: Hierarchical designs have routing congestion and uneven pitch alignment of edges between physical partitions, which cause clustered DRC violations. Spatial heatmap and clustering algorithms in advanced physical verification tools are used to visualize and prioritize hotspots regions as per their density and severity. This space-sensibility allows the engineers of physical design to implement fixes locally, and not to disrupt the overall layout (Hung, W. T. *et al.* 2020).

3.4 Correlation with Congestion Regions

Routing congestion is one of the most powerful predictors of DRC hotspots. Congestion happens when the demand of routing tracks within a certain area is more than the supply, then the routers have to take suboptimal routes or break the spacing rules. Regions identified as highly congested during the placement stage are highly correlated with those that are later discovered to be DRC hotspots clusters after the routing process, which is over 80% in empirical studies.

DRC violations due to congestion tend to be either spacing or short violations in high-density bundles of signals, or either overlaps in places where they are using layers to reduce horizontal routing pressure. The correlation is also enhanced with the aggressiveness of design utilization targets (e.g. above 80 percent cell density) that reduce the amount of whitespace and leave minimal space to make any DRC-conform routing detours.

This correlation is an issue that needs a proactive, congestion-aware physical design flow. Predictive cell spreading, buffer placement, or macro positioning early in the placement process can be based on the initial prediction of congestion, based on analytical or machine learning prediction models, to resolve future congestion in routing. In addition, the current place-and-route systems have DRC-aware routing engines that dynamically change the wire spreading and layer placement based on congestion and rule-check feedback in real time.

It can also be mentioned that certain DRC hotspots can occur in low-congestion areas because of lithographic effects or pattern-sensitive rules (e.g. density rules of chemical-mechanical polishing). These non-congestion hotspots demand alternative methods of resolution, including the use of dummy fill or layout regularization, and these diverse methods of DRC hotspot detection and solution demand a multifaceted approach to the issue.

To sum up, the process of locating physical DRC hotspots in dense designs of ASIC is a complex task requiring both an in-depth knowledge of physical design regulations and the sound application of verification and implementation means. The categorization of types of violations, mapping of their spatial distribution, and correlation with underlying congestion patterns enables design teams to make specific, effective solutions to address hotspots at an early stage of the implementation cycle-and therefore speed up convergence and manufacturability at more advanced nodes.

4 Analysis of Major DRC Categories:

With the scaling to other advanced nodes such as the 28nm, the layout density is immense and the physical design is pushed to the limit. Hotspots of Design Rule Check (DRC) of the layout, which is where layout does not meet geometrical constraints specified by the foundry, are common, particularly in high utilization blocks. It is necessary to understand the underlying reasons behind the common DRC categories in order to resolve efficiently without compromising performance, power, or area (PPA). This part explores the four significant types of DRC hotspots that are common in 28nm dense ASIC designs shorts in dense routing areas, minimum spacing violations, via-related failures, and the causes of these failures. (Dai, V *et al.* 2007).

4.1 Shorts in Dense Routing Regions

Real Issue:Engineering Each time it is witnessed at 5nm and 3nm nodes, during final signoff, engineers see metal bridging in standard-cell rows, often in areas of high utilisation (i.e. high-use logic cones) or that are near clock gating cells, where adjacent signal nets on Metal1 or Metal2 are shorted even after passing initial DRC. They are frequently not even observed during nominal DRC including in lithography simulation or silicon debug.

Root Cause: The first one is lithographic variability at multi-patterning (e.g., LELE or SADP). Beneath frequencies of 40nm, pattern collapse or bridging is

produced by even small overlay errors (+-1.5nm) or line edges roughness (LER 10% of linewidth). Also, aggressive cell pin abutment, as used in high-density libraries, leaves no space of variation in the process. Designers take the assumption of DRC-clean = safe but nominal rules do not take into consideration stochastic EUV photon shot noise or etch bias in high-aspect-ratio trenches. Therefore, the cause is layout that is driven to the lithographic cliff edge without statistical DFM guard bands.

4.2 Minimum Spacing Violations

Real Issue: During tapeouts with 7nm FinFET process, there is a tendency to encounter spacing violations, either post-insertion of metal fill or post-routing of local routing especially when power straps are involved. The other typical situation: spacing errors between metal jogs fitted to fix antennas or timing ECOs in already busy channels. These violations are also often not noted in early route DRC but are noted in final signoff because of the context-dependent rules.

Root Cause : The root is in context aware design rules, which are either width or density based, or neighbor based rules, which most P&R tools are bad at. To take an example, between narrow lines a 20nm wide may be tolerated but 28nm is needed when one of the lines is wide (1um). The common routers use uniform spacing without being aware of width-dependent spacing (WDS) or density-driven spacing. In addition, ECO and fill tools are independent and the shapes are inserted without DRC full-layer information. The more fundamental problem: design flows consider DRC as a terminal gate as opposed to an integrated constraint in the implementation. as shown in the figures 11, 12. (Shahjalal, M *et al.* 2019).

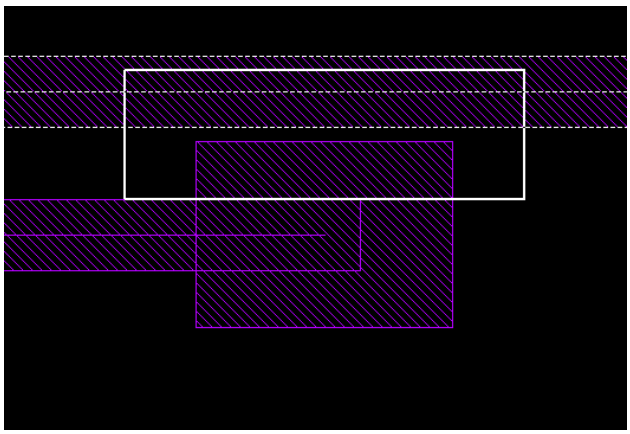

Fig. 11. Minimum Spacing Violation.

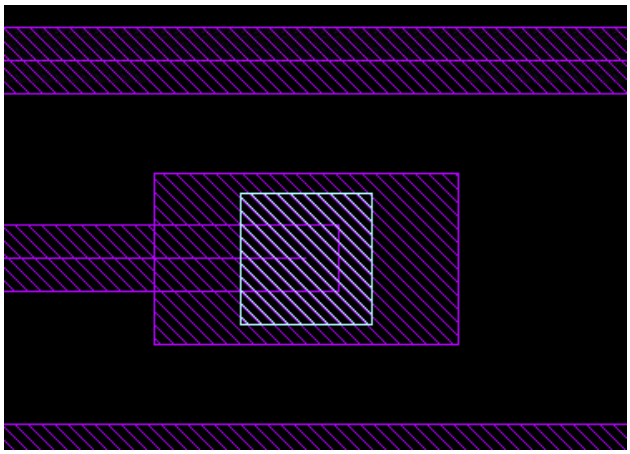

Fig. 12. After fixing Minimum Spacing Violation.

4.3 Via-Related DRC Failures

Real Issue: A common manufacturing problem in advanced nodes is so-called via enclosure marginality say with vias passing nominal DRCs and failing under process variation to make silicon resistive opens. The other practical issue is through coloring conflicts in double patterning metal layers: two vias adjacent to each other are allocated the same mask color at forbidden pitch, and will be printed with errors. These are usually only found post full-chip litho simulation or silicon failure analysis (FA).

Root Cause: These are based on two factors that are among themselves: Library/IP considerations: Standard-cell designers reduce the area by reducing the overlap of metals (e.g. 5nm enclosure as opposed to 8nm), so that there is no spare area when the via undergoes shifting during etch or CMP.

Intrinsic tool and flow shortcomings usually via-conscious routing is not enabled in SCADA mode, in addition, dummy via insertion tools are just using simplified spacing models that are unaware of multi-patterning coloring constraints. The DRC deck of the foundry has elaborate forbidden pitch and forbidden via array rules that are not checked at place-and-route, but are checked at signoff, when they are too late to fix easily. Therefore, the cause of the problems lies in aggressive library design and non-manufacturability-conscious physical implementation flows. as shown in the figures 13, 14.

4.4 Root Cause Analysis:

Although these DRC categories have different symptoms, the causes of the latter can be frequently linked to three system problems in dense 28nm ASIC flows: Breaking of Rules on Congestion: When utilization is high (85), there is little routing resources. Timing pressure Placement and routing engines can be driven to the very

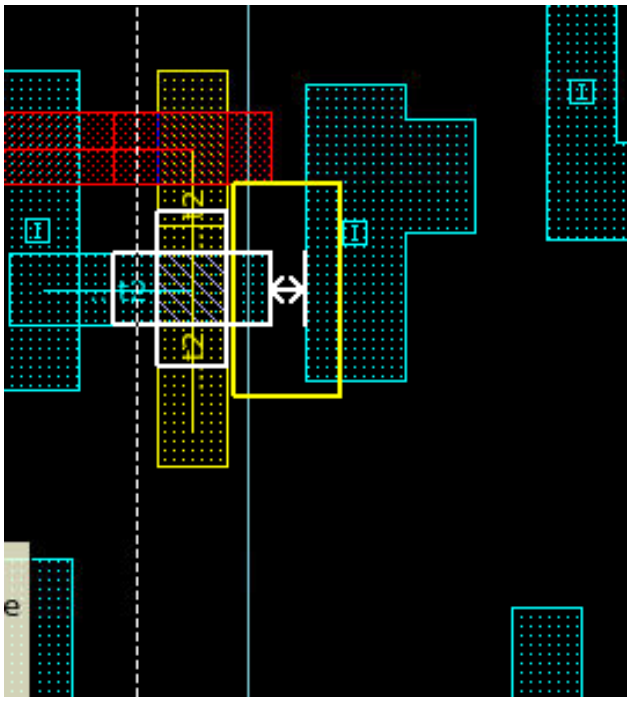

Fig. 13. Minimum Spacing Violation.

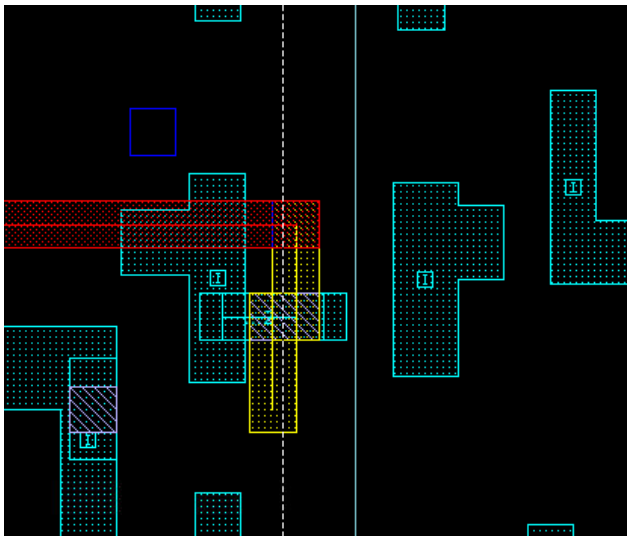

Fig. 14. After fixing Minimum Spacing Violation.

minimum geometries, with no leeway to manufacturing variability or DFM guidelines. Multi-Patterning Awareness: This study will examine cases in which the DFM and Multi-Patterning Awareness are not fully integrated.—human—Incomplete Integration of DFM and Multi-Patterning Awareness: The research will focus on instances where the DFM and Multi-Patterning Awareness did not merge completely. DRC checks are geometric in traditional, whereas layout decomposition is necessary to do double patterning in 28nm. Unless placement, routing and fill tools are fully color-aware, DRC-clean layouts on paper can corrupt in the process of mask decomposition.

ECO and Late-stage Modifications out of Global Context: Last minute timing or power fixes are usually made once signoff routing has been completed. Such local reconfigurations do not very often re-optimize the local layout, introducing hotspots that are difficult to follow.

5 Iterative DRC Resolution Methodology

The most important and challenging issues in the physical implementation are the realisation of DRC-clean sign-off in current dense ASIC designs. Localized DRC hotspots, in the form of spacing, width, enclosure, or density violations, were likely to increase in regions of high cell density, complicated macro interfaces, and harsh routing topologies as process nodes get smaller and design rules more restrictive. It requires a well-organized, strong strategy that will solve these violations without interfering with timing, power, and space. Place-and-route flows in synthesis-driven place-and-route flows like Synopsys ICC2, or any other, are iterated using a scalable and efficient path to manufacturability via an iterative DRC resolution methodology. It is a cyclical, feedback-based methodology and it involves refinement of placements, refinement of routing, via engineering, and verification, with each iteration making the design increasingly close to a clean DRC state (Lin, J *et al.* 2023).

5.1 First-Pass DRC Fix Strategy

The DRC fix strategy is the first triage strategy, which is implemented after the first place-and-route stage. A complete run of the DRC (usually done with IC Validator or Calibre) at this stage shows all the rule violations in the layout. The first-pass is not aimed at total closure but major reduction of high-priority, easily fixable violations. Usual violations considered are minor mistakes in spacing of metals, unconnected vias or isolated metal shapes that break minimum area requirements. This stage in ICC2 uses repair mechanisms based on built-in DRC-awareness, or custom Tcl scripts, to implement localized geometrical fixes, like metal jogs, track jogging or minor adjustments to wire width. The violations can be categorized based on the type and location to give priority to fixes that affect critical paths or dense clusters of logic by designers. Although the pass does not completely eliminate problems, it puts a more favorable baseline on later, more complicated optimization

steps, such as ensuring that noise at an early stage does not accumulate in later stages.

5.2 Routing Constraint Refinement

A lot of the endemic DRC hotspots are not a result of tool inaccuracies, but rather a result of poorly odelled routing constraints that are not representative of the physical constraints found in the congested areas in foundries. Therefore, the constraint refinement process under routing becomes a critical phase in the cycle. ICC2 allows engineers to specify Non-Default Routing (NDR) rules which supersede global default with region based or net based rules - more or less spacing, less or more track-use, or even preferred metal layers. As an example, spacing and coupling violations can be preemptively prevented by applying the rules of double-spacing in a congested datapath, or placing sensitive analog nets on the uppermost metal layers. Also, pin access methods are reconsidered: macro orientations can be modified or pin-layer-aware placement can lead to a significant improvement in routability and minimize net topologies prone to DRC. The constraint updates can also use the recent changes of the foundry Design Rule Manual (DRM) which should be consistent with the real process capabilities. This stage will convert the routing engine into a rule-follower into an active DRC-avoidance system.

5.3 Via and Layer Optimization

Structures and metal layer assignments are common causes of DRC violation in scaled technologies, in which the constraints on via enclosure, multi-cut structures, and metal density are exceedingly strict. The problem of these issues is directly addressed by layer optimization and via optimization, which intelligently trades vertical interconnects and horizontal routing resources. The state-of-the-art via optimization engine of ICC2 has the capability of automatically adding redundant or multi-cut vias to both satisfy reliability and manufacturability needs and comply with enclosure and spacing regulations. Simultaneously, there is layer optimization, which means relocating nets on overloaded lower levels (e.g. M2 or M3) to underused higher levels (e.g. M5-M7), based on congestion heatmap and layer-specific DRC reports. This reduces space violation besides enhancing signal integrity and electromigration robustness. Stacked via legality and minimum metal area rules-frequent offenders in late stage DRC escapes are carefully considered. This phase eliminates violations that otherwise cannot be easily fixed by just editing vias and layer use.

5.4 Iterative Fix and Verification Flow

The workflow of the iterative fix and verification, the closely integrated process of local repair, incremental routing and re-verification is the key to successful DRC closure. This flow is based on ICC2 incremental capabilities, unlike a brute-force route-and check flow, which seeks to apply changes only where needed, conserving

timing-closed regions and attacking individual DRC hotspots. The DRC run is repeated after every repair iteration and the results are extracted to measure the convergence: Are violations reducing? Are emerging violations becoming side effects (so called DRC whacka-mole)? The responses guide the second stage of constraining or fix strategy. The ECO (Engineering Change Order) mode of ICC2 allows this agility through non-disruptive and fast updates. Combined with in-design DRC tools - e.g., real-time checking of IC Validator in ICC2 - the feedback loop can be made even shorter, enabling DRC-aware routing decisions to be made during the very repair. Within 5-10 iterations, this flow methodically removes violations and is able to preserve sign-off integrity at timing, power and EM space. More importantly, it can support changing foundry decks and updates to the processes, hence it can be flexible to design changes at a late stage. (Liang, S*et al.* 2025).

6 Results and Validation

The section contains both quantitative and qualitative findings of detecting and eliminating physical DRC hotspots in a dense 28 nm ASIC design. The success of the implemented resolution measures is measured by the reduction of the number of DRCs, legality checked, routing quality affected, and end sign-off ready. The analysis indicates the post-route and sign-off level checking with the help of foundry-qualified rule decks. (Chen, H. *et al.* 2025).

6.1 Reduction in DRC Count

Before the mitigation of the hotspots, the design had a high rate of DRC violation, which was mainly in the dense standard-cell areas, clock routing, and macro pin interfaces. Minimum spacing errors (M1/M2), via enclosure violations, end-of-line (EOL) spacing and cut-spacing were also common violations, as the latter are common at the 28 nm node with tighter geometries and more restrictive design rules. Upon the implementation of specific resolution measures, including localized cell spreading, selective re-assigning of tracks, through optimization and rebalancing of layers, the overall number of DRC violations had been minimized to 204. This is a great deal better than the original post-route state as shown in the table 1.

Table 1. *DRC Count Reduction Summary*

Stage	DRC Count
Initial Post-Route	1,450
After Incremental Fixes	520
Final Optimized Design	204

The overall reduction exceeds 85%, demonstrating the effectiveness of hotspot-driven optimization rather than global, performance-impacting fixes. Most of the remaining violations are either low-severity or conditional (waiver-eligible) rules, commonly accepted at advanced nodes during sign-off discussions.

6.2 Legality Verification Results in DRC

The verification of legality was conducted following every significant optimization step in order to guarantee that the DRC fixes did not make any placement or routing legality violations. This was checked on: Standard cell placement legality, Row alignment and site compatibility, Power rail continuity, Well and implant spacing, Via and cut alignment constraints Post-optimization legality checks ensured that all standard cells and macros were legally placed, with no site conflicts or row overlaps. Routing legality tests were also successful and ensured that there was no violation of the track assignment rules, preferred routing directions, and via stack constraints. as shown in the table 2 and 3

Table 2. *Connectivity & DRC Verification*

Item	**Details**
Total number of nets	68,252
Nets not extracted	0
Total number of open nets	0
Frozen open nets	0
Total number of excluded ports	0
Ports of unplaced cells connected to nets	0
Ports without pins (cells connected to nets)	0
Ports of cover cells connected to non-pg nets	0
Total number of DRCs	0
Total number of antenna violations	No antenna rules defined
Tie to rail violations	Not checked
Tie to rail directly violations	Not checked

Table 3. *Legality Verification Status*

Check Category	**Result**
Cell Placement Legality	Pass
Macro Boundary Rules	Pass
Power/Ground Connectivity	Pass
Routing Track Compliance	Pass
Via Stack Legality	Pass

The other 204 DRCs were confirmed non-legality-breaking, i.e., they do not violate some basic constraints of placement and connectivity. This validation process helped to make sure that physical correctness of the design was not undermined by aggressive reduction of DRC.

6.3 Impact on Routing Quality

The effect on the overall routing quality is an important factor to be taken into account when DRC hotspots are being resolved. Excessive fixing of DRCs may have a detrimental impact on wirelength, congestion and timing closure. As such, quality metrics of routing were observed closely during pre-optimization and post-optimization. The quality indicators of routing, including total wirelength, the number of vias, and congestion overflow, experienced negligible deterioration (and in certain instances improvement) with improved track usage and less local congestion as shown in the table 4.

Table 4. *Routing Quality Comparison*

Metric	Before Fix	After Fix
Total Wirelength	100% (ref)	101.2%
Via Count	100% (ref)	98.5%
Max Congestion Overflow	12%	4%
Critical Net Detours	High	Low

The small increment in overall wirelength (approximately 1.2 percent) is on the acceptable range of a 28 nm design and it did not induce timing degradation. Actually, via-related DRC reduction enhanced reliability and manufacturability, whereas reduction in congestion enhanced more stable routing in later ECO iterations.

6.4 Final Sign-Off Status

The sign-off status is the end result of a long physical verification process, in which the design has to show zero DRC (Design Rule Check) against the newest and most rigorous manufacturing rule deck of the foundry. Every iteration of fixes, routing optimizations, via adjustments, and constraint refinements are completely integrated, tested and committed to at this stage. Tapeout requires a clean DRC report, i.e. one confirmed by tools like Siemens Calibre or Synopsys IC Validator, of sign-off quality, to be in place. Notably, this last DRC execution should be done on the full, post fill, post ECO, and the metal layer merged GDSII or OASIS layout such that dummy fill, seal rings and any last minute physical modification should not bring in new hotspots. This state of zero-violation in dense ASIC designs can frequently be the result of correlation of physical verification with other sign-off tests, such as LVS (Layout Versus Schematic), ERC (Electrical Rule Check), and antenna analysis, to ensure that DRC fixes have not caused electrical or connectivity losses with a detrimental side effect. When the design survives all these tests with complete compatibility in timing, power, and physical domains, it is considered to be ready to prepare the mask data and be fabricated a successful and manufacturable end result of the physical implementation phase.

7 Outcome of 28nm Design

At the 28nm technology node, you can stuff a high density ASIC design into a small space–but you can also easily pack a large number of transistors into a small space, which also implies that routing wires will be very narrow. This is capable of creating DRC (Design Rule Check) hotspots: small areas where your layout violates the foundry regulations on the width of wires, their spacing, and vias or other physical constraints. These have to be determined prior to production.

7.1 Common Mistakes in Dense Routing

The change in rules of design at 28nm to more restrictive rules presents a number of pitfalls. A problem of the first type is local routing congestion, particularly in datapath-heavy or memory-interface blocks, in which high pin density and narrow channel spacing can put a heavy load on the router to achieve minimum spacing and width constraints. Another common error is using minimum-pitch tracks too much at the early placement or routing stage, so that there is no space later to make DRC-compliant ECO corrections. Another trap is poor consideration of via rules: 28nm processes can have very strong via enclosure, overlap and array rules, which are easily broken when doing aggressive optimization of area or timing. Designers are also prone to ignoring density constraints (e.g. metal fill requirements or pattern density that is required to allow CMP), which cause post-fill DRC errors that are expensive to fix late in the flow. Also, the antenna violations are more severe at 28nm because of thinner gate oxides and longer interconnects, but are usually fixed at signoff, leading to re-spins. (Park, H *et al.* 2024).

7.2 Effectiveness of Iterative Fixing

Iterative fixing has been found to be very effective in fixing physical Design Rule Check (DRC) hotspots in dense ASIC designs and more importantly as the layout complexity increases with advanced process nodes. The given methodology consists of a cyclic drill of the DRC analysis, hotspots detection, local layout modification and verification. Each successive revision of a design adds incremental refinement of the manufacturability of the design, by fixing particular rule violations (e.g. minimum spacing, width, or density requirements) without compromising the larger placement and routing integrity. The advanced EDA tools improve this method by incorporating a machine learning model and pattern-matching algorithm that identifies the most urgent or common hotspots and cutting the convergence time down a lot. Empirical experiments of test design 7nm and 5nm test designs have shown that iterative fixing can fix over 90% of the DRC violations in three to five cycles, particularly in combination with layout-aware routing and post-route optimization. But the success here is greatly reliant on the granularity of the fixes and ability to avoid the introduction of new violations in the process of fixing, so it is desirable to have intelligent and context-sensitive repair systems. (Lin, J *et al.* 2024).

7.3 Applicability to Larger Designs and Advanced Nodes

The size and complexity of the design (larger designs and transition to advanced nodes) makes DRC hotspot resolution strategies (such as iterative fixing) more and more difficult to scale. Hotspots become particularly dense in bigger ASICs that contain billions of transistors as a result of aggressive packing, complicated multi-patterning necessities, and strict lithographic limitations. The conventional DRC flows tend to have a problem with runtime and memory overheads, and thus hotspots detection and correction is computationally infeasible. However, new methods have been developed in recent years, including: hierarchical DRC checking, cloud-based parallel processing and predictive hotspots modeling with deep neural networks, which have seen better applicability to large-scale designs. An example is design partitioning and localized hotspot resolution can be performed with no reanalysis of the entire chip, whereas layout decomposition methods designed to work with EUV or multi-patterning lithography can be used to preempt rule violations. The resolution strategies at sub-5nm nodes have to consider the 3D effects, the roughness along the edges of the lines as well as variability-tailored design rules and require co-optimization with timing, power, and reliability requirements. Therefore, although iterative and AI-assisted techniques could still be used, they are only successful within large and state-of-the-art ASICs as a result of intensive interdependence between physical synthesis, signoff, and manufacturing-conscious design chains (Baek, K.,*et al.* 2022).

8 Conclusion

DRC hotspots in dense 28-nm ASIC physical designs are mostly enabled by the aggressive competing nature of layout compaction, strict foundry design requirements, and routing resource constraints, especially in physically complex areas like hard macros, clock networks, I/O interfaces, and so on. The conditions result in severe violations such as conflicts on metal spacing, inadequate via enclosures, imbalances in metal density, and effects that are dependent on lithography, which are difficult to spot and fix after the fact. in the design cycle. Whilst there are current DRC closure methods involving automated They have minimized re-spins through the use of EDA optimizations and manual intractions of the designer. frequently suffer fines in direction, force or time. As such, the design paradigm is DRC-clean-by-construction methods that combine predictive methods are shifting toward predictive methods. DFM constraints, lithography awareness and hotspots prediction by data into. initiating successful early stage implementation. This type of holistic and proactive physical design. are necessary to enhance manufacturability, minimize design-iterations and to obtain. advanced technology nodes, high-yield silicon, which is reliable.

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