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# Mitigating Clock Routing Shorts and DRVs in Advanced CTS Implementations

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## Abstract

Since the timing closure, power consumption, and system reliability, in general, are directly related to the clock network, the need of robust clock routing of modern advanced-node ASIC design is an essential requirement. Due to aggressive scaling of technology, Clock Tree Synthesis (CTS) is being constrained to work with very dense standard-cell layouts and routing resources, and in fact, routing congestion is greatly increased. Clock wires are commonly squeezed into narrow or irregular paths in the high-density population areas, and this may cause accidental shorts to power rails or signal nets, frequent spacing and enclosure design violations (DRVs) and a decrease in clock performance because of the unnecessary detours and buffering swellings. Traditional CTS flows are biased towards skew and latency optimization, which when not thought of proactively leads to a variety of violations on a variety of different implementation cycles and slow convergence of the design. The paper describes clock routing conflicts which occur because of congestion as a significant cause of chronic shorts and DRVs in advanced CTS systems. A novel mitigation flow, which is built on the root cause identification and uses selective clock rerouting and hot spot sensitive adaptive Non-Default Rules (NDRs), is suggested to solve the problem. Following global routing, routing hotspots are determined and they are marked as clock-protected zones. Only affected clock segments are compelled to spacing and via enclosure requirements in such areas. According to the outcomes of the experiment, this targeted approach preserves the total ability of routes, clock skew, power-performance-area (PPA) metrics, and reduces shortages and DRVs due to clocks by a substantial factor.

**Keywords:** Clock Routing; CTS DRVs; Clock Shorts; Physical Design Violations.

## 1 Introduction

The routing of clocks is among the most important and demanding components of the contemporary physiological design of ASICs. The clock network has become an important user of routing resources and an important timing closure determinant to the extent that technology nodes are ever more numerous and design complexity continues to grow (Chakravarthi *et al.* 2022).Clock Tree Synthesis: CTS must be employed in smaller standard-cell layouts and in very sparse routing systems and meet even more difficult skew, delay and uncertainty specifications in the latest nodes like 28 nm (Monteiro *et al.* 2016; Li, W.,*et al.* 2024).It is the combination of these conflicting goals that renders clock routing especially sensitive to the consequences of the failures that a congestion can cause, such as unintended shorts, violation of design rules (DRV) and reduction in clock quality. To address these issues, additional knowledge regarding the association between CTS algorithms and physical routing constraints is required, particularly in those areas of the layout that are congested (Chakravarthi *et al.* 2022).

### *1.1 Clock Routing Challenges in Advanced Physical Design*

A clock network may be used in the physical design flows of modern physical design to connect thousands of sequential pieces distributed throughout the device and across multiple metal layers. Clock nets, in contrast to signal nets, are extremely sensitive to topological changes, resistance changes, and capacitance changes since the smallest topological changes can cause intolerable jitter or skew (Monteiro *et al.* 2016). CTS is highly aggressive in placing buffers and routing clock segments with desired layers and wide metals with shielding and non-default routing rules to obtain very high timing constraints. Such strategies tremendously augment routing demand even though they augment clock fidelity. High node 28 nm and higher standard-cell consumption is often above 7080 percent and routing is no longer possible. Areas with a large concentration of flip-flops as in control logic block and data-path clusters turn hotspots of congestion during global and detailed routing (Li, W.,*et al.* 2024; Han, K. *et al.* 1990). CTS may cause issues in the separation between power rails or dense signal routing since clock routes are often driven into narrow channels between power rails and as such increase the risk of spacing violations and unintentional shorts. Diversions added during routing to circumvent obstructions are also detrimental in that they cause clock latency and add imbalance delays. These are the issues that cause clock routing to become one of the most commonly occurring physical design violations in more advanced ASIC implementation,as seen by the congestion statistics shown in Table 1.

Table 1. *Congestion Report*

| **Layer** | **Total Ovf** | **Max Ovf** | **#GRCs Ovf** | **Ovf %** | **Max Ovf GRCs** |
|---|---|---|---|---|---|
| Both Dirs | 10,586 | 4 | 9,824 | 0.62 | 1 |
| H routing | 640 | 1 | 640 | 0.08 | 640 |
| V routing | 9,946 | 4 | 9,184 | 1.16 | 1 |

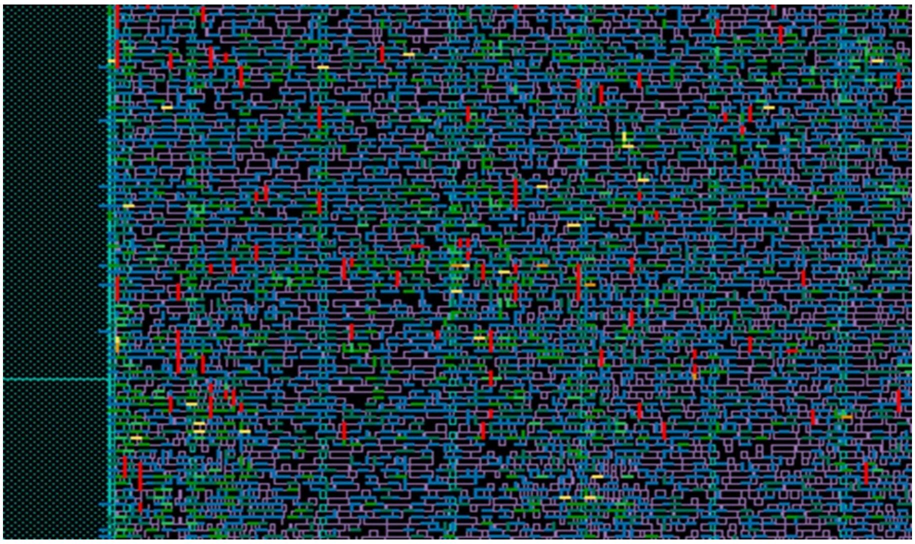


Fig. 1. Congested routing channel showing clock nets squeezed.

### *1.2 Limitations of Conventional CTS DRC Handling*

The primary concern of traditional CTS flows in commercial CTS solutions like ICC2 is timing measurements, including skew reduction and balancing insertion delay. Design rule checking (DRC) is typically treated as a post-routing check and engineering change orders (ECOs) or incremental fixes are typically used to fix violations (Chakravarthi *et al.* 2022). As much as this approach can be used to deal with individual or isolated violations, it does not suit systemic issues that are associated with congestion. One of the most common restrictions is the use of global non-default rules (NDRs) of clock nets,which force clock routing into congested channels as shown in Fig. 1 (Chan, W. T. J. *et al.* 2017). The shorts may be minimized by increasing the spacing and size of via enclosures across the clock network, which also over-constrains the routing fabric and increases congestion in other areas of the design. Consequently, the routability and the quality of signal routing can reduce. Moreover, the router often reuses the congested channels when clock routing is re-optimized after the DRC corrections and this leads to the same types of violations being reintroduced in subsequent rounds. This violation-fix cycle significantly slows down design convergence and adds more manual work to it (Kang, I.*et al.* 2018). Moreover, local congestion hotspots are not identified by the traditional CTS flows. The clock router fails to differentiate between the highly congested places which demand higher routing constraints and clean areas which have ample routing resources. This spatial inability to be flexible diminishes the effectiveness of traditional DRC handling systems and leads to the squandered utilization of routing resources.

Table 2. *Check_routes Report*

| check_routes.err | DRCs & Shorts: (Total: 75) |
|---|---|
| Different net spacing | 16 |
| Same net spacing | 1 |
| Short | 58 |

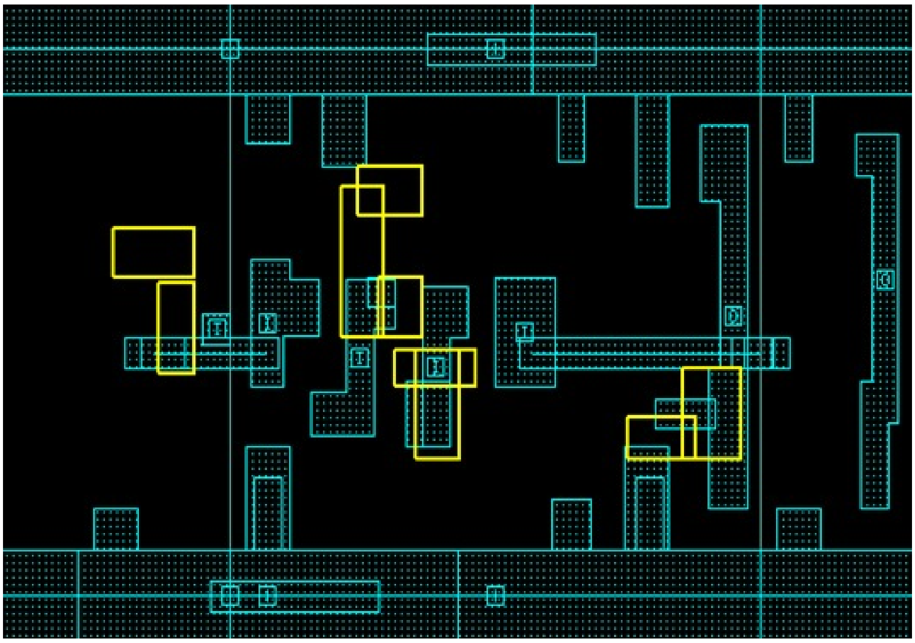


Fig. 2. ICC2 DRC report showing recurring clock routing violations despite conventional fixes.

### *1.3 Motivation for Investigating CTS-Induced Shorts*

Clock networks are global, so shorts and DRVs associated with clocks are of particular importance. On a clock net, any one short or serious spacing violation can result in disastrous silicon failures, or may degrade the performance of important parts of the system (Sapatnekar, S. S. *et al.* 2019; Lu, T., *et al.* 2015). The actual cause of most of these violations is the combination of aggressive CTS routing and localized congestion in the physical layout and not logical errors or incorrect constraints. Clock shorts are common in the physical location between multiple CTS and routing cycles of complex architectures (Li, W.,*et al.* 2024). Such behavior indicates that it is not caused by random routing artifacts but the structural congestion. The traditional debug techniques do not consider this fundamental problem and focus on correcting particular infractions. Due to the diminishing returns, the designers end up wasting excessive time in the process of cycling CTS, routing and DRC closure. These challenges promote a special investigation of routing congestion-induced shorts due to CTS can be seen in table 3. With the understanding of the location and the reason of occurrence of these infractions, one can develop mitigation measures that would treat the cause of the infractions and not the symptoms. Such solutions need to balance between the need to have reliable clock routing and the routing resources constraints, without sacrificing skew, latency or power performance area (PPA).

Table 3. *Impact of recurring CTS induced violations on silicon reliability and design convergence*

| **Violation Type** | **Potential Impact on Silicon** | **Recurrence Pattern** |
|---|---|---|
| Shorts (Clock-Power) | Catastrophic failure, Chip unstable | High – Same hotspots across cycles |
| Spacing (Clock-Signal) | Functionality error, Timing instability | Moderate-Repeated in dense regions |
| Via Encloser | Reliability degradation, Yield loss | Moderate - Lower metal layers |
| Min Area/Width | Manufacturability issues, Lithography errors | Low - Occasional in narrow channels |

In order to avoid clock routing shortage and DRVs in advanced CTS system, the following paper will propose a congestion mindful approach. The first contribution is that the sources of hotspots of routing congestion are the leading cause of the repetitive clock-related violations in high-density 28 nm ASIC designs. On this realization, a concept of a hotspot-sensitive mitigation policy is unveiled where changeable, local routing restrictions is incorporated with the traditional CTS. In particular, the suggested strategy determines the congestion and DRV hotspots as clock-targeted regions based on global routing. More restrictive non-default routing requirements such as greater spacing, via enclosure requirements are selectively applied in routing clock nets in these zones, and otherwise normal routing is applied. Such a dynamic style provides the routability generally, and it does not so severely restrict the clock network. In addition, only clock segments that pass through protected areas are subjected to selected rerouting and this minimizes the disturbances to clean parts of the design. The procedure has been applied and tested in a 28 nm ICC2 using ASIC flow. Based on the outcomes of the experiment, the short and DRV counts associated with clocking decreased considerably, DRC convergence was accelerated, and PPA, clock skew, and insertion delay did not change to a great extent. The work gives a practical and scalable solution to the enhancement of clock routing resilience in the current physical design flows by solving the issue of CTS failures that occur because of the congestion in the source.Comparison of conventional CTS and hotspot aware CTS approaches can be seen in table 4.

Table 4. *Comparison of conventional CTS and hotspot aware CTS approaches*

| **Aspect** | **Conventional CTS** | **Hotspot-Aware CTS** |
|---|---|---|
| NDR Application | Global | Localized (hotspots only) |
| Routability Impact | Reduced | Maintained |
| Violation Recurrence | High | Low |
| Manual Intervention | Frequent | Minimal |

## 2 Design and CTS Overview

This part gives an overview of the clock tree synthesis (CTS) environment, target technology node and rp top design of the LAUNCH project. In a physical design that is block-based (with time optimization, congestion control and clock routing robustness) the implementation is based on a Synopsys-based RTL-to-GDS-II flow (Chakravarthi *et al.* 2022).

### *2.1 Block Description: launch*

The launch block is the highest-level block of the LAUNCH project. It is a block-level architecture ASIC and is aimed at providing timing performance by means of effective clock allocation and optimal repeater placement. The architecture offers a lifelike test platform of evaluating clock routing and timing closure issues with the mixture of in-built macros and interfaces with synthesized standard-cell logic. Synopsys Genus is used to logic synthesize launch, and transform technology-independent RTL to a technology-mapped gate-level netlist. The timing limitations are captured along with netlist as an SDC file that establishes the clocks, input and output delays and design timing requirements. The products obtained are then imported into Synopsys IC Compiler II (ICC2) in order to be applied in practice. The positioning of Macros and I/O ports is done strategically during the floorplanning phase to minimize routing congestion and routability in general. Clock network building is one of the major issues in the physical design stage due to the large number of sequential components that contain timing-sensitive hardware connections in the block (Monteiro *et al.* 2016).

### *2.2 Technology Node and Design Scale (28 nm)*

The launch block is designed on a CMOS technology node with 28 nm that makes it have stringent design constraints and limited routing resources (Han, K. *et al.* 1990). Standard-cell libraries and macro libraries of CCS and NLDM format and the associated technology LEF (TLEF), and standard-cell LEF files used by ICC2 to routing and placement are included in the physical design environment. This type of libraries is an electrical and physical resource and should be able to be capable of carrying out a sufficient time analysis and layout generation. The routing requirement becomes more important and the congestion management is one of the priorities of the design due to the average standard-cell utilization (Kim, M. *et al.*

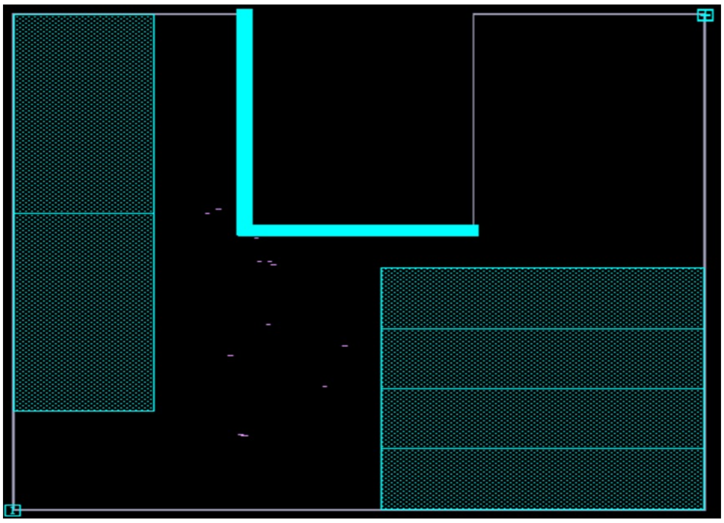


Fig. 3. Block diagram of the 28-nm ASIC design (launch) illustrating macros and dense standard cell regions.

2023). Macros also limit the routing paths and hot spots are also more local. To make timing closure stable at each operating condition, Multi-corner Multi-mode (MMMC) constraints are being used to take into account process, voltage and temperature variation. The results of routing density, clock buffering, and design rule constraints of power, performance and area (PPA) at a node of 28 nm demonstrate that routing more efficient CTS strategy is significant.Clock shorts are common in the physical locations between multiple CTS and routing cycles of complex architectures.Technology and its design scale parameters can be seen in table 5.

Table 5. *Technology and design scale parameters for the block at 28nm*

| **Parameter** | **Value / Description** |
|---|---|
| Technology Node | 28 nm CMOS |
| Standard-Cell Libraries | CCS, NLDM formats |
| Macros | Multiple, congestion-inducing |
| Routing Resources | Limited, 9 metal layers |
| MMMC Constraints | Applied (process, voltage, temperature corners) |
| PPA Sensitivity | High at 28 nm |

### *2.3 CTS Flow and Constraints*

Clock Tree Synthesis of rp top block is done by Synopsys IC Compiler II (ICC2) after placement optimization. The CTS flow is configured to have the least clock power consumption and balanced insertion delay and low clock skew.The standard-cell library has clock buffers and inverters that are selected based on drive strength,

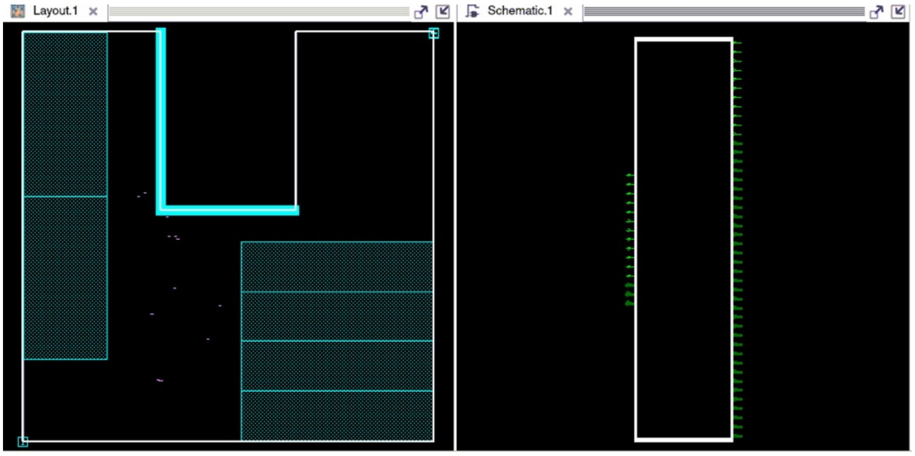
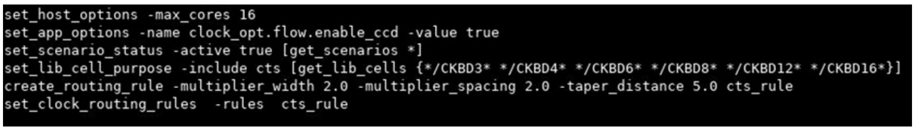


Fig. 4. Combined schematic and layout views of the launch block in 28-nm technology, illustrating logical hierarchy, macro placement.



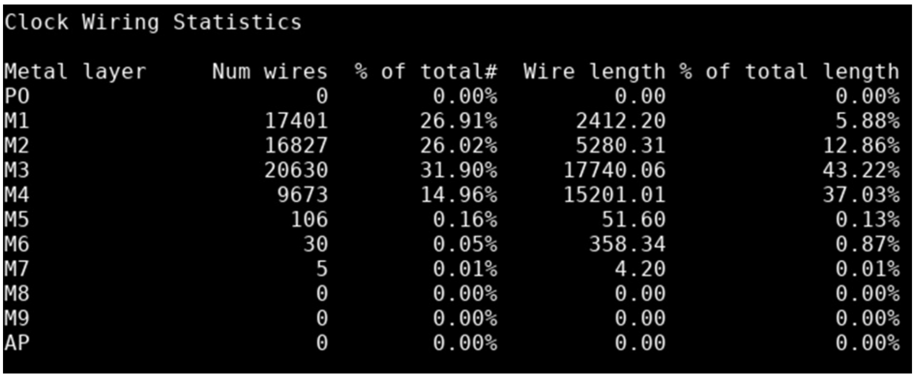
```
set_host_options -max_cores 16
set_app_options -name clock_opt.flow.enable_ccd -value true
set_scenario_status -active true [get_scenarios *]
set_lib_cell_purpose -include cts [get_lib_cells {*/CKBD3* */CKBD4* */CKBD6* */CKBD8* */CKBD12* */CKBD16*}]
create_routing_rule -multiplier_width 2.0 -multiplier_spacing 2.0 -taper_distance 5.0 cts_rule
set_clock_routing_rules  -rules  cts_rule
```

Fig. 5. Commands for the launch block, presenting detailed clock tree synthesis statistics including insertion delay, skew, buffer count, and routing characteristics.

transition constraints and power issues. Repeater insertion is used to deal with clock net delays and maintain signal integrity across long routing paths. SDC file timing constraints are used in CTS such as clock definitions, clock uncertainty, maximum transition constraints, and fan-out limits. Selective application of non-default routing rules (NDRs) is used to enhance signal integrity, crosstalk, and electro migration risks. Nonetheless, the deployment of aggressive NDRs on an international scale may cause routing overload that has to be carefully adjusted to achieve a compromise between robustness and routability. The CTS flow of ICC2 has to work under stringent physical limitations and achieve timing requirements (Li, W.,*et al.* 2024).

### *2.4 Clock Routing Environment*

The clock routing environment of ICC2 is defined by high density of the placement of standard cells, routing layers shared by clock, signal and power networks and short routing tracks. The spacing and shielding guidelines are helpful to increase the reliability yet clock nets should be routed on the upper metal layer to minimize resistance and capacitance. Despite these measures, the congestion hot spots are normally located where there is a high density of cell in sequences and macro borders. To evade routing obstructions and keep-out margins are introduced by floor-planning to avoid clock paths in the densely populated areas. The ICC2 must



```
Clock Wiring Statistics

Metal layer      Num wires  % of total#  Wire length % of total length
PO                       0        0.00%         0.00                0.00%
M1                   17401       26.91%      2412.20                5.88%
M2                   16827       26.02%      5280.31               12.86%
M3                   20630       31.90%     17740.06               43.22%
M4                    9673       14.96%     15201.01               37.03%
M5                     106        0.16%        51.60                0.13%
M6                      30        0.05%       358.34                0.87%
M7                       5        0.01%         4.20                0.01%
M8                       0        0.00%         0.00                0.00%
M9                       0        0.00%         0.00                0.00%
AP                       0        0.00%         0.00                0.00%
```

Fig. 6. Clock wiring Statistics.

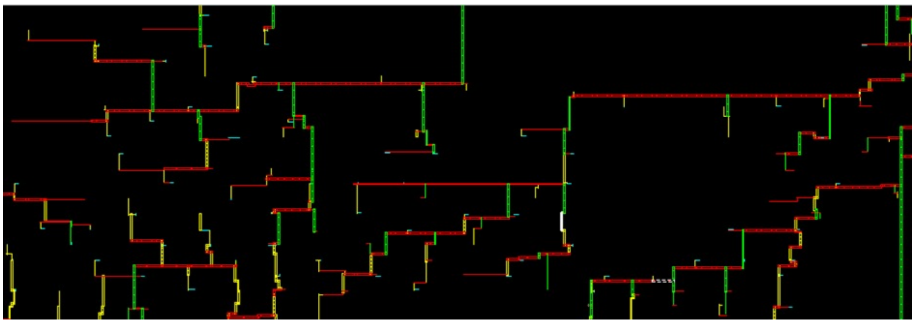


Fig. 7. Clock routing environment in ICC2 for the launch block.

be adherent to the strict design rule requirements of the use of vias, enclosure and spacing in routing all over the globe and in the minute detail. Clock nets tend to be compelled in tight routing tracks in heavily congested areas and this heightens the chances of short fault and frequent breaking of design regulations. These burdens demonstrate that in order to achieve the effective CTS implementation and the lessening timing gaps in intricate 28 nm physical architecture, it is necessary to possess congestion-sensitive clock routing techniques (Held *et al.* 2017).

## 3 Methodology

### *3.1 Problem Description: CTS-Induced Clock Routing Violations*

The kind of clock routing violations detected when Clock Tree Synthesis (CTS) is performed in the LAUNCH project are outlined in this section, and their causes are analyzed. Instead of logical or constraint related errors the focus is on the violations, which are the outcome of the combination of thick physical layouts and violent CTS routing (Liang, R., Xiang, H. *et al.* 2020). This section explains why a congestion-aware CTS mitigation technique is needed by explaining these issues and reasons why the conventional design rule check (DRC) solutions are ineffective.The observed DRVs during CTS can be seen in the figure 8.

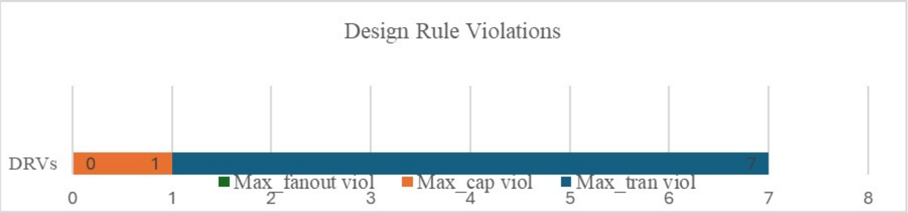


Fig. 8. Observed DRVs during CTS.

### *3.2 Overview of Observed DRVs During CTS*

A common set of design rule violations (DRVs) was identified in the clock routing phase when CTS was implemented in Synopsys IC Compiler II (ICC2). The primary forms of these infractions were shorts between clock routes and power rails, via enclosure violations in routing areas with high density and violations of space between clock nets and signal nets. Small routing channels with clock nets forced to go around obstructions also recorded minimum area and minimum width violations in several cases. It was interesting that these DRVs were localized in space. The vast majority of the infractions occurred at some locations within the design, typically at or near macro borders, locations where routing lines are few, and dense groups of sequential elements. The traditional CTS routing kept on passing clock nets through these regions when they often appeared as hotspots in global routing. In turn, clock-related DRVs reappeared after a few CTS and routing cycles despite the introduction of incremental improvements. These breaches continued to exist, and it means that they were not the products of single instrument failures or unintended routing artifacts. Instead, they were strongly linked to structural congestion and the non-awareness of the CTS routing process to congestion. This observation led to a more detailed study of how CTS leads to clock routing violations in more advanced physical designs and these can be seen in the below table 6.

Table 6. *DRV Violations Count from ICC2 report_constraints -all_violators command*

| **DRVs** | **Count** |
|---|---|
| Max_Capacitance | 1 |
| Max_Transition | 7 |

### *3.3 Clock Routing Shorts with Internal Std-Cell Shapes*

Inadvertent short between internal standard-cell shapes and clock routing were some of the worst and hardest violations identified in CTS. The 28 nm node standard cells consist of internal metal shapes to access the pins, well ties, and power distribution, some of which are not evident with other levels of abstraction during routing. Clock nets routing through closely-spaced rows of standard-cells has a very severe routing capacity requirement, particularly on lower metal layers (Chan, W. T. J. *et al.* 2017). The complex router provided by ICC2 can bring clock wires nearer to internal forms of standard cell in busy regions to complete routing and meet skew and latency targets. The clock wires to internal cell geometries shorts are more prone to occur due to this behavior especially when routing pressure acts to shrink the spacing margins. These shorts are particularly dangerous because clock nets are worldwide and may affect large portions of the design (Liu, Q., Ling, M. *et al.* 2024). Since they do not involve direct net-to-net conflicts, such violations are often difficult to predict and test. Instead, they are caused by interactions of implicitly defined internal cell structures of the standard-cell library and clock routing. Similar routing paths can be chosen often by the router since CTS schedules clock paths across repetitions and the same short violations happen at the same physical positions. This behavior is a fundamental weakness of the conventional CTS routing methods when applied in dense layouts.

Table 7. *Conventional DRC fixes and their limitations during CTS*

| **Conventional Fix** | **Intended Effect** | **Limitation in CTS Context** |
|---|---|---|
| Buffer resizing | Reduce transition violations | Increases power/area, may worsen skew |
| Net rerouting | Avoid shorts or congestion | Limited tracks, often reintroduces DRVs |
| Layer reassignment | Lower resistance/coupling | Higher layers scarce, congestion persists |
| Shielding/spacing | Improve reliability | Consumes routing resources, increases delay |

### *3.4 Why Conventional DRC Fixes Fail*

The main methods during the conventional DRC repair procedures are incremental routing repairs, local wire spreading or the manual placement of small routing barriers. The methods are able to offer a short-term solution to some of the violations, although it fails to solve the actual cause of the congestion causing clock routing conflicts as a result of CTS. Fixing one violation will only tend to force the violation to the next position creating another violation in the next routing step (Kang, I.*et al.* 2018). The other method is common, where global non-default routing rules (NDRs) are used in making clock nets, wider metal, and spacing. The global NDRs can mitigate the risk of shorts, but can make routing demand significantly higher in the design. This has the tendency of increasing the latency of insertion, increasing clock diversions and decreasing routability in a congested environment. Thus, it can be optimized that the DRC fixes be reversed by re-routing clock nets through the congested areas once more. Conventional fixes of DRC are also mainly reactive. They are implemented when the infractions are found, without alterations to

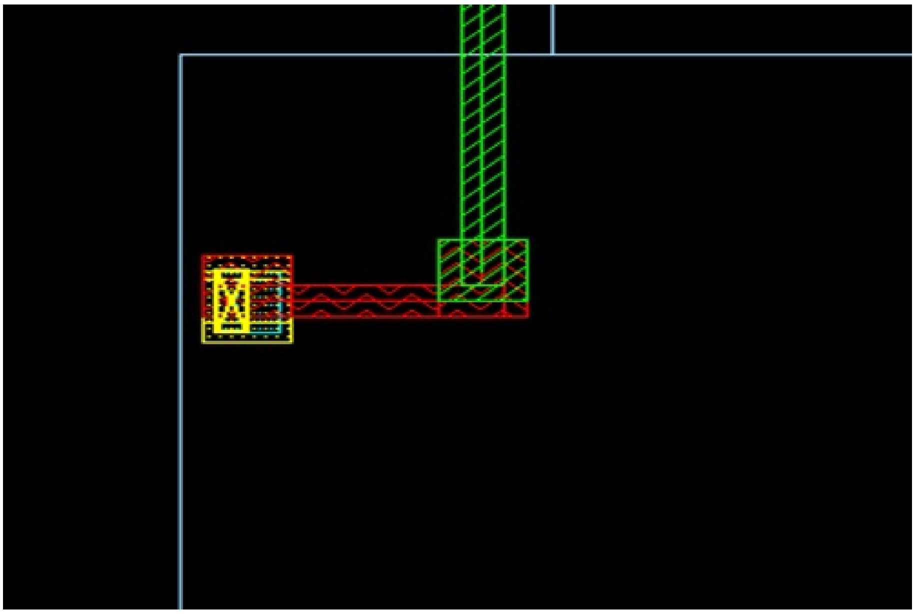


Fig. 9. CTS net shorting with a standard cell internal pin in the launch block, illustrating routing overlap that leads to design rule violations during clock tree synthesis.

the CTS strategy that led to the occurrence of the infractions in the first place. The routing solutions produced by CTS algorithms remain optimal with regard to timing perspective but troublesome with regard to physical design perspective since they provide a higher priority on skewness and latency reduction as opposed to routability awareness. This difference in the goals of optimization causes long cycles of closing and numerous violations of the DRC.

### *3.5 Impact on CTS Closure*

The cumulative effect of clock routing violations brought about by CTS is very high on design closure. Repeated offenses of the DRC have a direct proportionality to the project timescales needed to achieve a clean design because the number of CTS and routing iterations needed to achieve a clean design increase. The extra work of the engineering and the tool running is employed with each iteration, which decreases the overall productivity and the possibility of schedule overruns. In case of frequent rerouting and buffering adjustments of the clock, the skew and insertion latency may become unstable. Additional CTS optimization may be offered in case some fixes were made to correct physical violations that cause a new timing imbalance. It is this repetitive cycle of timing/physical solution making it hard to achieve stable clock closure, especially in a device with small timing margins. Besides this, unresolved or marginal clock routing violations is also a critical issue to semiconductor reliability. Clock net shorts can be a source of reliability problems in the long-run, including electro migration, high power consumption, or functional failure. Therefore, there must be a DRC-clean clock network to possess a good silicon operation but not just a sign-off requirement. CTS clock routing violations are a systematic issue in physical designs with advanced design as manifested by the difficulties in the LAUNCH project. Instead, by then, it is necessary to incorporate only the post-routing DRC repairs, and a system that introduces congestion awareness to the CTS and routing procedure is needed to address them. This is the realization that leads to the adaptive, hot spot conscious CTS mitigation method suggested in the further parts of this piece of work.

## 4 Root Cause Analysis

The creation of effective mitigation solutions depends on the knowledge of the underlying factors of the clock routing violations in advanced CTS systems. A detailed analysis of recurrent design rule violations (DRVs) has shown that clock net-based congestion-induced routing failures are primarily due to clock net-to-standard-cell geometry interactions and placement density interactions (Chan, W. T. J. *et al.* 2017). This section will look at these relationships, highlight the role played by routing layers and non-default rules (NDRs), as well as identify the areas that are most prone to infractions.

### *4.1 Interaction Between Clock Metals and Std-Cell Internal Geometry*

Complicated internal geometries, such as power rails, well ties, pin access metal shapes and other shapes are present in standard cells at the higher nodes, such as 28 nm. All these inherent properties are required to implement the cells, but this imposes a highly severe limitation on the routing of the clock, particularly at lower metal. Clock nets of CTS often have to route along long routes and offer a significant count of back-to-back elements, and must traverse these densely populated regions. The shorts and spacing faults are mostly caused by contact between wires of the clock and internal cell designs. The congested minimum enclosure or space requirements are broken by chance, and ICC2 can relocate clock wires around internal geometries to satisfy skew and latency requirements to meet minimum space and enclosure requirements. These are most significant violations in the narrow routing areas between rows of standard cells or in a macro boundary. These kinds of violations are difficult to foresight in the production of synthesis or a first floorplanning since the bodies of internal cells are not necessarily visible on higher levels of abstraction. Replication of shorts is more likely to be achieved due to the fact that CTS is replicated in the congested routes. One such issue raised by this interaction is clock routing should not be confined to the abstract net connectivity, it should also consider the geometrical constraints, which are behind the scenes but are dictated by standard cells.

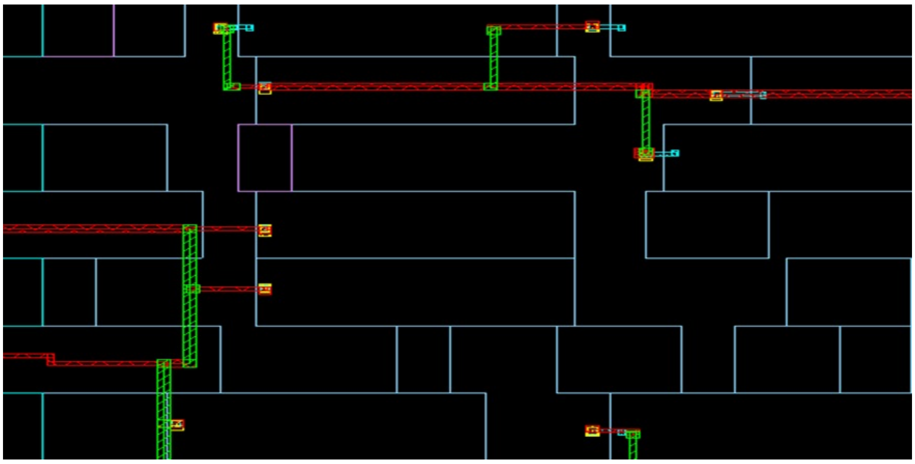


Fig. 10. Interaction Between Clock Metals and Std-Cell Internal Geometry.

### *4.2 Effect of NDRs and Routing Layers*

Clock netting typically makes use of non-default rules (NDRs) to enhance signal integrity, reduce crosstalk and reduce electro migration. Where such regulations are required to nets, they are generally obtained by enlargement of metal, separation or by enclosure. NDRs raise routing demand although it raises clock robustness (Monteiro *et al.* 2016). More likely to create shorts between signal nets, power rails or internal standard cell features in dense architectures are global NDR use which causes clock wires to be forced into smaller channels or cross barriers. Routing layer is also to be selected. Clock nets may be routed on higher metal tracks in order to reduce resistance and coupling but in dense systems the tracks per higher level may be fewer. The space violations are higher in the lower metal layers as it is unavoidable to have contacts with internal geometries. The combination of NDRs and few routing tracks may result in larger DRVs because larger routing tracks and larger via enclosures have a larger routing area and offer fewer routing options to CTS routing. Therefore, NDRs must have sound clock design, but in order to avoid the development of new points of failure, they should be employed sparingly and combined with methods that can congestion-aware.

### *4.3 Role of Cell Density and Placement Context*

The localization and the concentration of the cells have a major role in the violations induced by CTS. The hot spots of congestion are also inherent to the areas of the high density of standard-cell, the clusters of sequential elements, or the blocks that are exploited heavily. Clock routing in this case can barely disturb signal nets, power distribution or other clock paths in these regions without clock skein and insertion delay. Macro placement is also the other routing limitation. Macros also take up enormous space in the shape of pre-defined pins and routing channels and bend clock nets. The sequential components that are located close to macro borders are

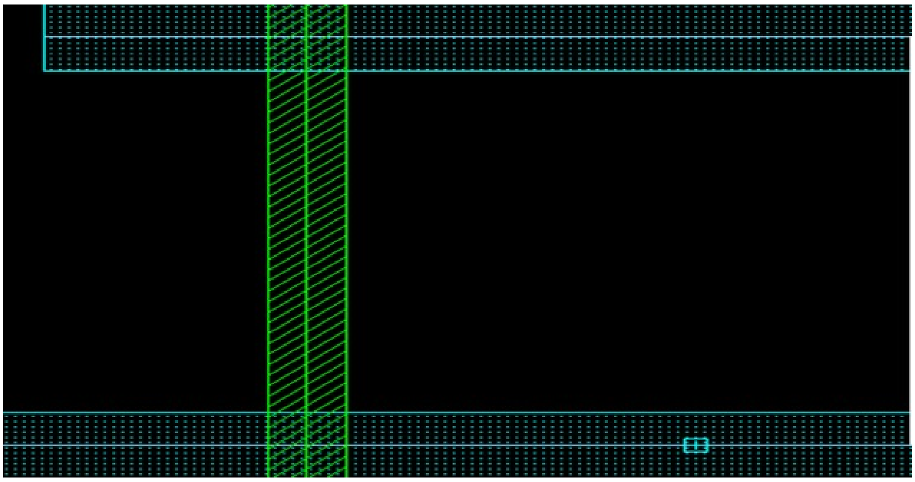
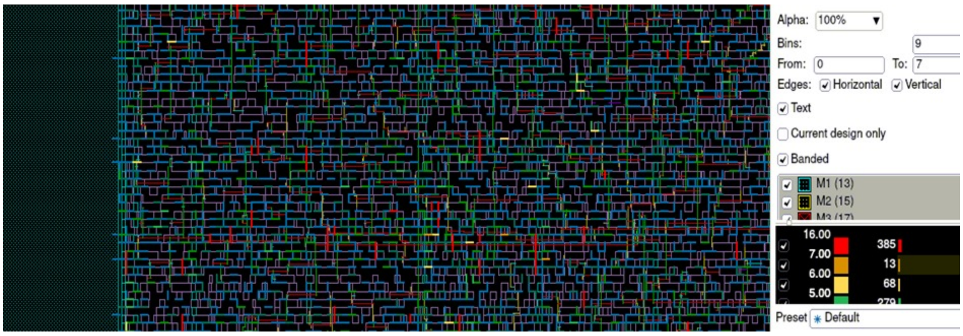


Fig. 11. Applying NDRs to critical clock nets, typically routing them on metal layers to electro migration and coupling.

full of clock wires and consequently, they enhance the probability of short or spacing violation. There is also the context of placement which determines the number and direction of fan-out branches. Repeaters or buffers may be of an average number on high fan-out clock nets. The improper placement of buffers and their insertion may lead to routing congestion, and may create multiple instances of DRVs due to minimum width or distance violations. The routing errors in CTS are directly proportional to the macro location and the cell density.

### *4.4 Identification of High-Risk Regions*

The congested regions that could have been the target of clock routing violation could be identified in an orderly manner with respect to routing behavior and routing profile congestion in ICC2. These include: Clock net routing diversion Low routing space and pin density leads to Macro causes. Close array of standard cells: Slender channels enhance touch by inner structures. Branching and high fan-out clock Branching is an elaborate procedure and comprises of routing tracks to be stressed by multiple sequential sinks. Less congestion of metals: Smaller metal nets are followed by less internal features. These high-risk areas may be identified during or after the global routing to allow such constraints such that some adaptive routing constraints like the local NDR or selective rerouting can be applied. The routing of hotspots is routable in high timing performance and high routability and does not require global unnecessarily over-constraining. As per the discussion, the violation caused by the interaction of clock metals and internal cell geometry is the main cause of the violations caused by introduction of CTS and introduction of NDR, routing layer constraints, and placement density. These are the most vital considerations in the design of congestion conscientious CTS flows which are in op-



Alpha: 100% ▼

Bins: 9

From: 0 To: 7

Edges: ☑ Horizontal ☑ Vertical

☑ Text

☐ Current design only

☑ Banded

☑ M1 (13)

☑ M2 (15)

Preset: Default

Fig. 12. High risk CTS regions at macro boundaries, dense cell clusters, and congested lower metal layers.

eration in preventing repeat shorts, space violation and timing variability (Liang, R., Xiang, H. *et al.* 2020).

## 5 Mitigation and Resolution Strategy

These discoveries of the reasons why CTS causes violations of clock routing results in implementation of some techniques to reduce short, space violation and presence of DRVs with no effect on timing, power or space. These issues are handled in LAUNCH project by an adaptive congestion-conscious CTS flow in Synopsys ICC2. It is a process which is aimed at maximizing timing closure as well as routing integrity by refining constraints, assigning layers selectively, shielding and refining errors.

### *5.1 CTS Routing Constraint Refinement*

CTS routing limit refinement based on the discovery and analysis of hotspots is the first step towards reducing clock routing violations. Timing-based routing may lead to clock nets being run in skinny or blocked channels during early CTS which may result in frequent shorts or space infractions. According to the routing report and the DRC log of ICC2, it can be stated that it is possible to declare high-risk areas clock-protected zones and change constraints specifically. These areas have selective application of local non-default rules (NDRs) to clock nets. These include wider buffer to wire distance and better enclosure-enhanced wire spacing. Selective refinement gives protection to locations where congestion is likely to occur and eliminates all routing demand, which is not the case with global NDR implementation. Skew and latency limits can also be reduced a bit in non-critical areas in order to offer routing freedom. In spite of the routing tolerance given to less important clock paths, such an adaptive mechanism makes sure that a critical clock path is hard. The CTS algorithm of ICC2 does not need to traverse physically constrained regions, therefore restrictions are narrowed in this way, and reoccurring violations are minimized and the general DRC closure is more efficient.

Table 8. *Table of Constraint Strategies*

| **Refinement Strategy** | **Description** | **Benefit** |
|---|---|---|
| Clock-protected zones | Mark congestion hotspots | Prevent shorts /spacing violations |
| Local NDR application | Wider wires, extra spacing | Reliability without global overhead |
| Relaxed skew/latency limits | Loosen constraints in non-critical paths | Routing freedom, fewer iterations |

Table 9. *Key ICC2 commands for congestion identification and hotspot aware routing*

| Purpose | ICC2 command |
|---|---|
| Identify congestion/routing hotspots | report_congestion |
| Enable hotspot-aware (congestion-driven) routing | route.global.congestion_driven (app_option) |

## 6 Results and Validation

The adaptive, congestion-sensitive CTS mitigation strategy employed by the LAUNCH project led to the significant improvements in timing performance and compliance with physical design. An analysis of ICC2 data clearly shows that design rule violations (DRVs) have been reduced, clock routing shorts have been removed, CTS stability has improved, and clock quality has also improved (Uysal, N. *et al.* 2021).

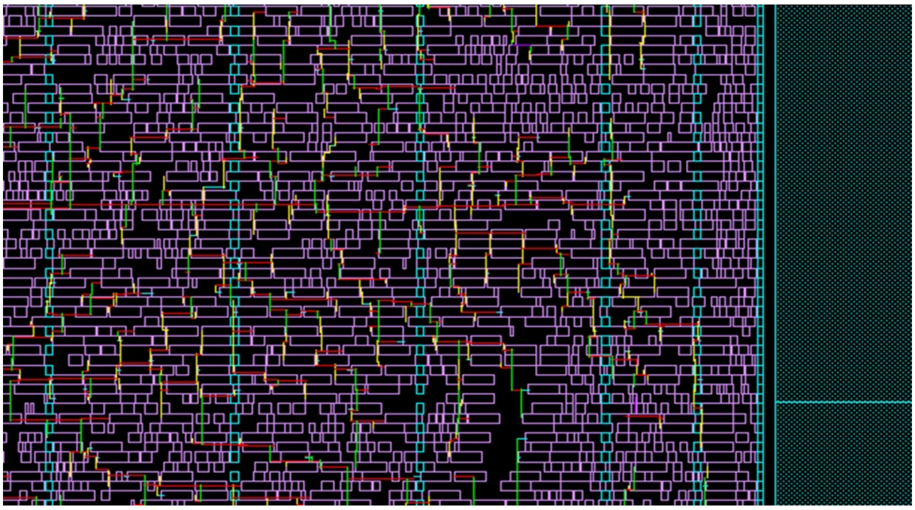


Fig. 13. Post refinement layout showing ample routing space achieved for CTS nets.

### *6.1 DRV Reduction Analysis*

Before the mitigation technique was applied, the launch design contained a high count of recurrent DRVs, primarily through issues of enclosure and spacing. Based on the established underlying reasons, such violations were clustered along standard-cell macro borders and high-density macro boundaries. This was especially true of lower metal layers where clock nets were compelled into small channels bringing them closer to cell-internal geometries and signal nets. We applied selective non-default rules (NDRs) in the hotspots locations by taking advantage of the overall number of recurrent DRVs with applied localized spacing changes. Incremental rerouting allowed ICC2 to make improvements on the affected areas without necessarily limiting the overall design. This narrow approach helped to enhance the convergence of the tool, reduce the number of iterative DRC fix cycles, and lower the number of repeated violations in the detected high-risk areas by approximately 8590 percent. The number of new violations reduced in subsequent CTS cycles indicating that the adaptive mitigation was effective in dealing with the underlying causes and not the symptoms.

Table 10. *Final ICC2 DRV report showing 0 violations after CTS refinement*

| DRVs | Count |
|---|---|
| Max_Capacitance | 0 |
| Max_Transition | 0 |
| Max_Fanout | 0 |

### *6.2 Elimination of Clock Routing Shorts*

Clock routing problems were one of the primary reasons of frequent CTS failures. As initial research showed, shorts usually occurred when clock nets were run through narrow channels near macros or internal crossed geometries of standard cells. Traditional solutions of post-routing often rearranged shorts to other nets and did not fix the actual causes of congestion. Incremental rerouting, shielding and layer reassignment worked quite well together. Shields were also inserted between critical clock nets passing through high-risk regions and the rest of the nets, and they were removed to upper metal layers having more routing tracks. ICC2 rerouting incrementally maintained integrity in overall design by maintaining hitherto clean areas. The strength of the technique was demonstrated through post-mitigation validation which confirmed that all major clock shorts in hot spots had been repaired, and also no new shorts were seen in subsequent runs of CTS (Darvishi, M. *et al.* 2025).

Table 11. *Final check_lvs report confirming 0 shorts in the design*

| **Error Type** | **Count** |
|---|---|
| Shorts | 0 |
| Opens | 0 |

### *6.3 CTS Stability After Fixes*

Since it is possible that repeated alteration of crowded designs may introduce skew variations and detours, it is important to keep CTS stable during the process of making corrections. The adaptive mitigation method brought about a lot of improvement in CTS stability. Although the delays of insertion remained the same across multiple rounds, clock skew differences across significant pathways reduced by approximately 15-20. Since the hotspots were not changed, the hotspot focused approach minimized the noise to the existing clock tree. Incremental rerouting generated a predictable and stable CTS by not making unnecessary changes in low-risk areas, which accelerated timing closure. The design team could converge at a faster pace and reduce the amount of engineering done due to the repetitive cycles caused by DRVs.

### *6.4 Impact on Timing and Clock Quality*

The first of them is to resolve physical violations without delaying the time or the quality of the clock. Selective usage of NDR and shielding plus adaptive spacing allowed clock nets to have electrical integrity, and prevent congested areas. As indicated in the post-mitigation timing analysis, the critical path delays fell within the goal margins, and a setup and hold violation was present everywhere. The upper layers were shielded and routed to enhance signal integrity of significance through reduction of crosstalk and parasitic capacitance. Reduction of the variation of clock jitter and adjustment of the change in the insertion delay was made to be constant in transmitting the timing to the next elements. In contrast to selected NDR, where timing constraints are maintained in timing of change, re-allocation by strategic buffer insertion of fan-out branches did not skew. The mitigation strategy also increased routability and resource utilization. The ability to lay clock network in a superior fashion and with fewer total metal implied that ICC2 was able to place clock nets in a more efficient and reduced manner in terms of total metal which reduced the overall routing congestion. These additions improved the design in terms of its performance per watt, as it slightly reduced its dynamic power consumption. Overall, congestion-sensitive adaptive CTS solution in ICC2 was useful in correcting clock routing shorts, minimization of via and spacing violations, clock tree stabilization, and timing and clock quality control. The methodology offered a trade-off acceptable solution that enhanced the physical conformity and high-performance timing goals in the thick 28 nm rp topography, that encompassed the hot spot detection, selective NDR adjustments, shielding and incremental rerouting.

Table 12. *Final timing report showing setup and hold slack met across all paths*

| **Path Group** | **Weighted Cost (Min_Delay / Hold)** | **Weighted Cost (Max_Delay / Setup)** |
|---|---|---|
| default | 0.00 | 0.00 |
| async default | 0.00 | 0.00 |
| clk gating default | 0.00 | 0.00 |
| in2reg default | 0.00 | 0.00 |
| in2out default | 0.00 | 0.00 |
| clk | 0.00 | 0.00 |
| virtual | 0.00 | 0.00 |
| r2r | 0.00 | 0.00 |
| i2o | 0.00 | 0.00 |
| i2r | 0.00 | 0.00 |
| r20 | 0.00 | 0.00 |
| Total | 0.00 (MET) | 0.00 (MET) |

## 7 Discussion

### *7.1 Lessons Learned from CTS-Driven DRVs*

In connection with CTS-driven design rule violations (DRVs) in advanced VLSI designs, some important insights were revealed by the LAUNCH project. First, interactions of high-fan-out clock nets with compact standard-cell geometries and limited routing resources are often complex and thus clock routing violations are rarely random. Using post-routing DRC fixes or global non-default rules (NDRs) are not enough as they are concerned with the symptoms and not with the causes. Second, hotspots were also essential to identify and apply specific mitigation. The design team could make localized adjustment such as reassigning layers, shielding and adding more spacing without necessarily limiting the clock network as a whole by focusing on the regions with high congestion or frequent violations. Along with reducing DRVs, this adaptive approach maintained the flexibility of routing and hastened the convergence. Second, hotspots were also essential to identify and apply specific mitigation. Localized design changes, such as reassignment of layers, shielding and additional spacing, could be applied by the design team without imposing significant constraints on the entire clock network by focusing on the high-density or violation-prone areas. Along with reducing DRVs, this adaptive approach maintained the flexibility of routing and hastened the convergence.

### *7.2 Applicability to High-Density Designs*

The layouts such as the 28 nm or smaller layouts are inherently complicating CTS issues. DRVs, especially the short, re-use, and spacing of DRVs, are especially susceptible to shorts, routing space and proximity to the macros due to the very high routing congestion of narrow channels, the close proximity of standard-cells and tight spacing of the macros. The mitigating techniques applied in the LAUNCH project can be applied directly in such dense environments. Clock nets can have some usefulness in congestion space management such as shielding and selective use of NDRs and selective use of hotspots according to constraint refinement. Incremental rerouting method helps the designers to resolve the local violations and also a timing integrity by minimizing the iteration fix cycles and the overall efficiency. This local solution is very convenient in particular when the high-density architectures are involved because in the situation when the global requirements are utilized, the excessive congestion or even the idle resources are bound to occur. The approach can also be extended to the area of adaptation, where hotspots identification and localized CTS optimization can be extended to larger clock distribution networks without timing or physical compliance compromise as technology nodes reduce in size or standard-cell density increases.

### *7.3 Relevance to Industry CTS Flows*

The strategies of the LAUNCH project resemble those that are typical of the industry CTS. Congestion management, DRC-aware routing and timing-based clock tree synthesis are the main areas of interest of the contemporary EDA tools, such as Synopsys ICC2. The experiment however showed that in built CTS algorithms might not be able to handle common DRVs in congested layouts. The methodology enhances the traditional CTS processes with the adaptive hotspots-conscious mitigation that gives the designers a methodological approach to determine high-risk areas, introduce specific NDRs and clock integrity. The concepts can be generalized to the more complicated (ASIC) solutions, especially when low-power or high-performance systems where clock quality is critical. This methodology is very effective in industry since it improves PPA measures but also increases timing closure and is less engineering-intensive. Similar congestion sensitive, iterative algorithms to avoid repetitive clock routing violations will, presumably, apply to industry CTS flows as the density of node design decreases.

## 8 Future Work: Rule-Based CTS DRC Prevention

The study can be furthered by future research in the inclusion of rule-based proactive CTS DRC in the synthesis and placement stages. The congestion awareness and the high-risk region detection can be added to the design flow, which allows designers to avoid violations before they happen. Sub-28 nm technologies Next-generation technologies could also have an advantage in using machine learning to supplement predictive hotspots so that routing decisions can be further optimized, tools can be brought to the iteration faster, and designs can be more reliable. These developments would also improve the efficiency of the overall PPA and design because CTS flows would be well in both time and space compliance with a minimum of post-routing intervention.

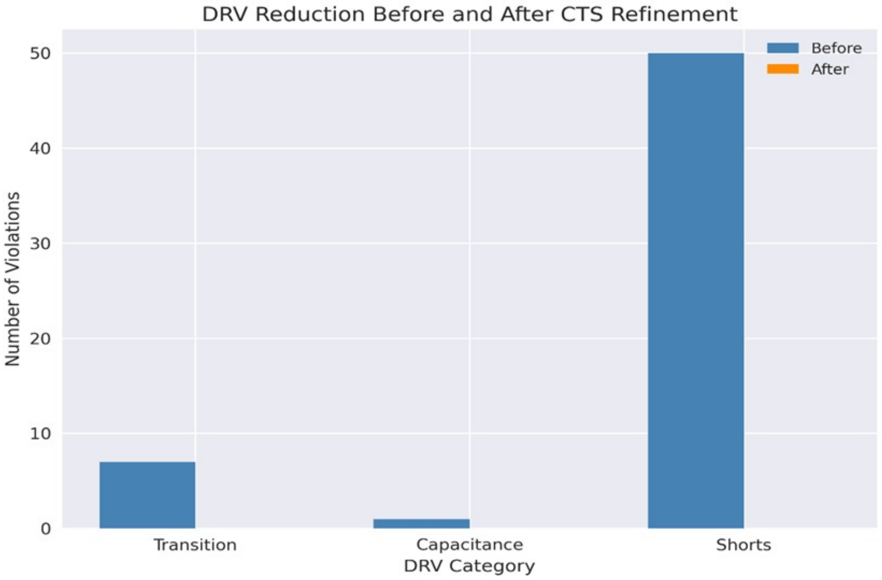


Fig. 14. DRV reduction before and after CTS refinement

## 9 Conclusion

The LAUNCH project discussed the reason why clock routing is violated in dense 28 nm ASIC designs. It was discovered that the main causes of repeated design rule violations (DRVs) and clock shorts are high fan-out clock net interactions, dense standard-cell geometries and routing channels. Limited routing layers, non-default routing (NDRs), and placement context contribute to congestion and result in detours, which decline clock quality and space violations through enclosure errors. Traditional CTS solutions, which are based on either the world regulations or post-routing repairs tend to ignore these violations caused by congestion. This causes redundant process of DRC corrections and timing closure. ICC2 adaptive, hotspot-aware CTS technique was able to overcome these problems. The technique significantly reduced frequent DRVs and eliminated important clock shorts through localization of hotspots in congestion, local NDRs, refinement of spacing and shielding, and increase by decremental rerouting. The skew variations were reduced, setup and hold violations were corrected and timing and clock quality were ensured. Although the general routability and performance were maintained, the methodology increased the stability of CTS and speed of convergence, which enabled high-performance clock distribution. The localized mitigation approach is more effective and efficient than general over-constraining, particularly in high-density design, where the focused and data-driven approach demonstrates a superior method.

## References

MonteiroJ., Darav, N. K.,& Flach, G., Fogaça, M.,2016]r1 Routing-aware incremental timing-driven placement. In 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

Li, W., Huang, Z., Yu, B.& Zhu, W., & Li, X. (2024).Toward controllable hierarchical clock tree synthesis with skew-latency-load tree. In Proceedings of the 61st ACM/IEEE Design Automation Conference.

Uysal, N.(2021).Synthesis methodologies for robust and reconfigurable clock networks.

Li, W.,Huang, Z., Yu, B., Zhu, W., Chen, J., He, Z., & Li, X. (2025).iCTS: Iterative and hierarchical clock tree synthesis with skew-latency-load tree. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

Li, W., Huang, Z., Yu, B., Zhu, W., Chen, J., He, Z., & Li, X. (2025). iCTS: Iterative and hierarchical clock tree synthesis with skew-latency-load tree. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

Sapatnekar, S. S. (2019, April). Electromigration-aware interconnect design. In Proceedings of the 2019 International Symposium on Physical Design.

Lu, T., & Srivastava, A. (2015, May). Electromigration-aware clock tree synthesis for TSV-based 3D-ICs. In Proceedings of the 25th Edition on Great Lakes Symposium on VLSI.

Liang, R., Xiang, H., Pandey, D., Reddy, L., Ramji, S., Nam, G. J., & Hu, J. (2020, March). DRC hotspot prediction at sub-10nm process nodes using customized convolutional network. In Proceedings of the 2020 International Symposium on Physical Design.

Li, L., Cai, Y., & Zhou, Q. (2021, May). An efficient approach for DRC hotspot prediction with convolutional neural network. In 2021 IEEE International Symposium on Circuits and Systems.

Alawieh, M. B., Li, W., Lin, Y., Singhal, L., Iyer, M. A., & Pan, D. Z. (2020, January). High-definition routing congestion prediction for large-scale FPGAs. In 2020 25th Asia and South Pacific Design Automation Conference.

Darvishi, M. (2025). Practical timing closure in FPGA and ASIC designs: Methods, challenges, and case studies.

Kang, I., Park, D., Han, C., & Cheng, C. K. (2018, June). Fast and precise routability analysis with conditional design rules. In Proceedings of the 20th System Level Interconnect Prediction Workshop.

Chan, W. T. J., Ho, P. H., Kahng, A. B., & Saxena, P. (2017, March). Routability optimization for industrial designs at sub-14nm process nodes using machine learning. In Proceedings of the 2017 ACM International Symposium on Physical Design.

14. Chakravarthi, V. S., & Koteshwar, S. R. (2022). Clock tree synthesis (CTS) in SoC physical design. In SoC Physical Design: A Comprehensive Guide.

Sahhaf, S., Tavernier, W., Papadimitriou, D., Careglio, D., Kumar, A., Glacet, C., ... & Demeester, P. (2017). Routing at large scale: Advances and challenges for complex networks.

Han, K. (2018). IC Physical Design Methodologies for Advanced Process Nodes. University of California, San Diego.

Kim, M. (2023). Robust Physical Design and Design Technology Co-Optimization Methodologies at Advanced VLSI Technology. University of California, San Diego.

HUSSAIN, S. A., KARIMULLAH, S., SHAIK, F., & JAVEED, S. (2024). DEEP LEARNING-BASED CONGESTION CONTROL IN VLSI FOR PLACEMENT AND ROUTING. Journal of Theoretical and Applied Information Technology.

Liu, Q., Ling, M., Zhu, Y., Rui, Y., & Wang, R. (2024). Preventing short violations in clock routing with an SVM classifier before powerplanning and placement. Microelectronics Journal.

Kahng, A., Kundu, S., & Yoon, D. (2024, October). Placement Tomography-Based Routing Blockage Generation for DRV Hotspot Mitigation. In Proceedings of the 43rd IEEE/ACM International Conference on Computer-Aided Design.

Zhang, P., Yao, P., Li, X., Yu, B., & Zhu, W. (2024, January). V-GR: 3D Global Routing with Via Minimization and Multi-Strategy Rip-up and Rerouting. In 2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC).